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(71) Déposant *(pour tous les États désignés sauf US)* : **STMICROELECTRONICS SA** [FR/FR]; 29, boulevard Romain Rolland, F-92120 Montrouge (FR).

(72) Inventeurs; et
(75) Inventeurs/Déposants *(pour US seulement)* : **MAZZONI, Simone** [FR/FR]; 2, Place Des Tilleuls, F-38000 Grenoble (FR). **CAME, Hélène** [FR/FR]; 30, rue Humbert II, F-38000 Grenoble (FR).

(74) Mandataire : BUREAU D.A.CASALONGA JOSSE; 8, avenue Percier, F-75008 Paris (FR).

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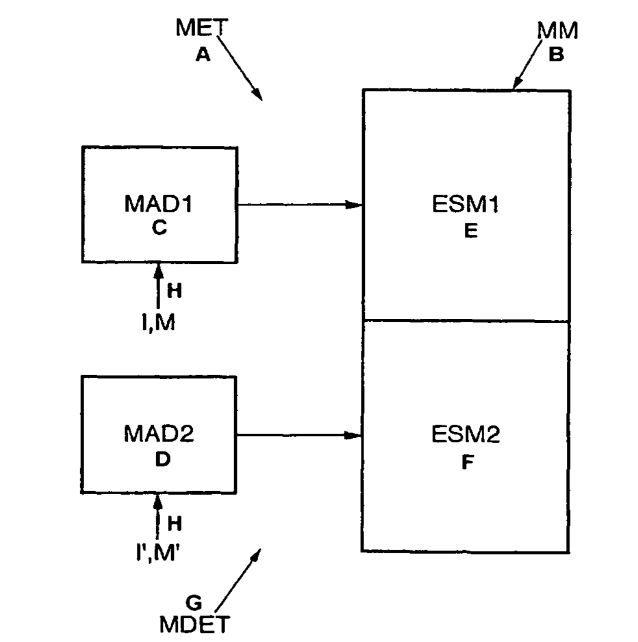
[Suite sur la page suivante]

(54) Title: DEVICE FOR TRANSMITTING/RECEIVING DIGITAL DATA CAPABLE OF VARIABLE-RATE PROCESSING, IN PARTICULAR ON A VDSL ENVIRONMENT

(54) Titre : DISPOSITIF D'EMISSION/RECEPTION DE DONNEES NUMERIQUES CAPABLE DE TRAITER DES DEBITS DIFFERENTS, EN PARTICULIER DANS UN ENVIRONNEMENT VDSL



A...INTERLEAVING MEANS
B...STORAGE UNIT
C...ADRESSING MEANS 1
D...ADRESSING MEANS 2
E...MEMORY WORKSPACE 1
F...MEMORY WORKSPACE 2
G...DEINTERLEAVING MEANS
H...PARAMETERS

(57) Abstract: The invention concerns a digital data transmitting/receiving device capable of processing different rates selected from a group of predetermined rates. It comprises a coding/decoding stage including interleaving means (MET) and deinterleaving means (MDET) comprising a storage (MM) whereof the minimum size is fixed in accordance with the maximum rate of said group, and having a first memory workspace (ESM1) allocated to the interleaving means and second memory workspace (ESM2) allocated to deinterleaving means. The size of each of said two memory workspaces are parameter-adaptive according to the rate being actually processed by the device.

(57) Abrégé : Le dispositif d'émission/réception de données numériques est capable de traiter des débits différents pris parmi un groupe de débits prédéterminés. Il comprend un étage de codage/décodage de canal comportant des moyens d'entrelacement (MET) et des moyens de désentrelacement (MDET) incluant une mémoire (MM) dont la taille minimale est fixée en fonction du débit maximal dudit groupe, et possédant un premier espace-mémoire (ESM1) alloué aux moyens d'entrelacement et un deuxième espace-mémoire (ESM2) alloué aux moyens de désentrelacement. La taille de chacun de ces deux espaces-mémoire est paramétrable en fonction du débit effectivement traité par le dispositif.

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En ce qui concerne les codes à deux lettres et autres abréviations, se référer aux "Notes explicatives relatives aux codes et abréviations" figurant au début de chaque numéro ordinaire de la Gazette du PCT.

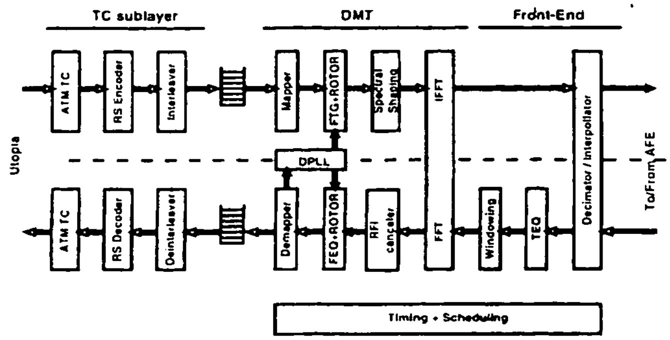

Figure 14.6.1: Chip block diagram.

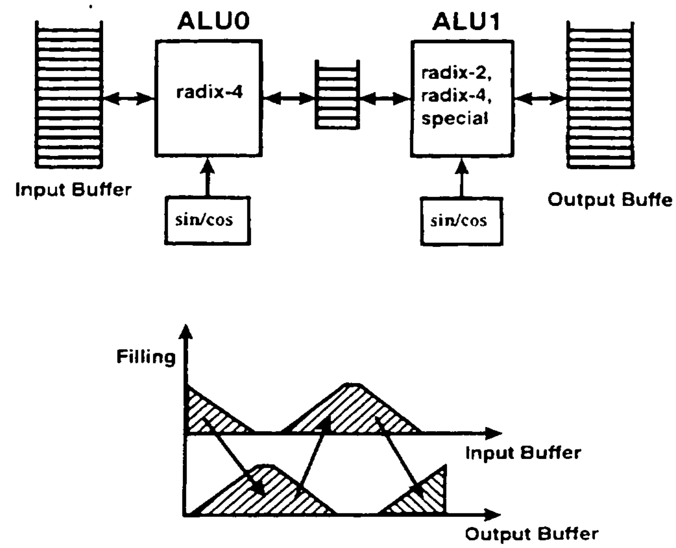

Figure 14.6.2: FFT architecture.

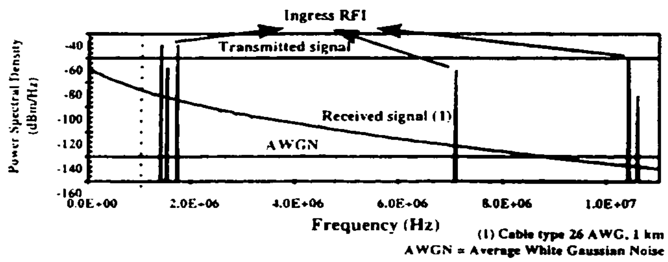

Figure 14.6.3: RFI noise characteristics.

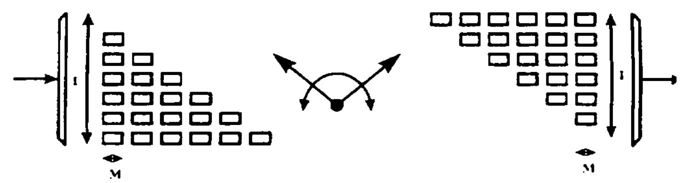

Figure 14.6.4: Interleaver.

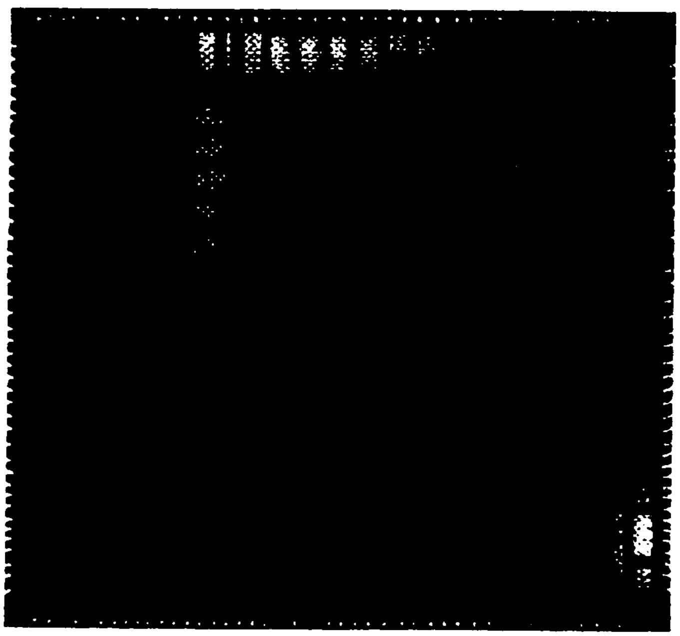

Figure 14.6.5: VDSL chip micrograph.

Technology	0.35 μm 5-metal CMOS
Gate	680k
RAM	900kbit
Frequency	44.16 MHz
Area	150 mm²
Package	PQFP-208
Transistors	9.0M
Power dissipation	2.7 W at 3.3 V

Table 14.6.1: Chip characteristics.

FFT	ALU1	ALU0
pass 1	bypass	radix-2
pass 2	radix-4	radix-4
pass 3	radix-4	special butterfly

IFFT	ALU1	ALU0
pass 1	bypass	special butterfly
pass 2	radix-4	radix-4
pass 3	radix-4	radix-4

Table 14.6.2: FFT and IFFT ALU usage.

XP-000862325 p.248-249 = (2) V8172

TP 14.6 A 70Mb/s Variable-Rate DMT-Based Modem for VDSL

Daniel Veithen, Paul Spruyt, Thierry Pollet, Miguel Peeters, Stijn Braet, Olivier Van de Wiel, Hugo Van De Weghe

Alcatel Bell, Antwerp, Belgium p.d. 02-1999

Very high-speed digital subcriber line (VDSL) technology can deliver data at multi-Mbits/s over the unshielded, twisted pair in overlay to the plain old telephone service (POTS) and ISDN services [1,2]. Discrete multi-tone (DMT) is one candidate for the modulation of VDSL. The DMT transmit signal is the sum of independent quadrature amplitude modulated (QAM) carriers spread over a bandwidth of 11.04 MHz. Time division duplexing (TDD) is used to provide a half-duplex communication channel over a single pair [1,2]. This chip integrates the complete digital signal processing required by a TDD-DMT VDSL system and the Transport Convergence (TC) sublayer functions such as (de)interleaving, Reed-Solomon (de)coding, (de)scrambling, (de)framing and the ATM-specific TC functions (Figure 14.6.1). It can be used both at the Network Termination (NT) and the Line Termination (LT) side.

DMT modulation and demodulation is by an FFT/IFFT block. This block performs a 512 points real FFT in less than 20µs. The FFT/IFFT is decomposed in complex radix-2, radix-4 and special resolve butterflies to combine results of the real FFT [3]. The block is based on a dedicated pipelined dual ALU. ALU0 can perform radix-4, radix-2 and special resolve butterflies. ALU1 needs only perform radix-4 operations (Figure 14.6.2). ALU1 is therefore 20% less complex than ALU0. To perform a complete 512 point real FFT, input data are read from the input buffer, pass ALU1, are temporarily reorganised in a small scratch buffer, pass ALU0 and are stored in the output buffer. This process is repeated twice and the final result is available in the output buffer (Figure 14.6.2). Table 14.6.2 summarizes the configuration of both ALU for the IFFT and FFT during the 3 passes. Data and twiddle coefficients are coded as floating point with 13 bits mantissa and 4 bits exponent, avoiding the use of block floating point with intermediate scaling between the radix [4]. Using a bit-true C++ model, optimum bit length for each intermediate stage of the ALU is derived. Simulations have shown that the noise generated by the FFT/IFFT block is well under the noise level of the VDSL system in the most favorable configuration.

In the front-end receive part of the chip, a variable rate decimator is followed by a variable rate Time Equalization (TEQ) block implemented as a FIR filter with programmable coefficients. The length of the TEQ can be programmed from 1 to 32 taps depending on the application. In the transmit path, a variable rate interpolator shares the same hardware as the decimator, due to the TDD scheme.

The hardest noise encountered in VDSL system is radio-frequency interference (RFI). Its power spectral density is typically well above the received signal (Figure 14.6.3). A programmable digital RFI canceller works in the frequency domain [5]. The RFI noise can be detected on 4 predefined frequency bands for each DMT symbol. The interference of two simultaneous RFI on the neighboring carriers can be reduced. The same floating-point format as for the FFT/IFFT block is used here to cope with the data dynamics encountered in the presence of RFI. A windowing is performed on the samples in the time domain, just before the FFT. Combining this windowing with the digital RFI cancelling yields an interference reduction of 45dB on the neighboring carriers.

Symbol timing recovery uses a digital phase-locked loop (PLL). This DPLL can be programmed to be of the second order or the third order with a bandwidth ranging from 0.1Hz to 100Hz, depending on the location of the chip in the system. The phase difference between receiver and transmitter clock is measured at the Demapper block and filtered out by a proportional-integral filter and then integrated to produce a value used to perform a digital rotation on each carriers in the frequency domain in both transmit and receive paths (Figure 14.6.1).

A slave Utopia interface provides the chip with ATM cells. Scrambling, header error control (HEC) generation and Idle cell insertion can be applied in the transmit direction. In the receive direction, basic ATM cell functions like cell synchronization, payload descrambling, idle/unassigned cell filtering and cell header detection and correction are provided.

A fully programmable Reed-Solomon (RS) encoder protects against random and burst errors. The number of check bytes can be programmed from 0 to 16 Band the number of data bytes can be programmed from 2 to 255B. An interleaver protects against error bursts by spreading the errors over a number of RS code-words. It is a triangular interleaver, with parameter I ranging from 1 to 255 and parameter M ranging from 1 to 34 (Figure 14.6.4). In the receive part, a programmable RS decoder and a deinterleaver perform the opposite transform. The parameters ranges are the same as for the transmit side. Two on-chip 32kB RAMs are provided to support the full parameter range for the interleaver and deinterleaver.

For some services, a constant data delay is mandatory, even if the bit rate on the line is changing. Therefore, the parameters of the interleaver/deinterleaver and RS encoder/decoder can be modified during normal operation of the chip, without any interruption or error generation. The synchronization between transmit and receive (of two different chips) is guaranteed by counting on both ends the number of transmitted and received RS code-words [6].

All the blocks of the chip can be separately bypassed for debugging. A central block, the Timing Unit, is responsible for chip synchronization of the chip and proper sequencing of operations.

A complete bit-true C model of the chip is available. The chip processes a 70Mb/s data stream coming from or going to the Utopia interface.

A buffer-tree used for clock distribution reduces power dissipated by the clock network. The characteristics of the chip are described in Table 14.6.1. A micrograph of the chip is available in Figure 14.6.5.

Acknowledgements:
The authors thank F. De Meersman and H. Fabri for contribution to chip layout.

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(71) Applicant:
ALCATEL ALSTHOM COMPAGNIE GENERALE D'ELECTRICITE
75008 Paris (FR)

(72) Inventor: **Peeters, Miguel**
B-1200 Brussels (BE)

(74) Representative: **Narmon, Gisèle**
Alcatel Bell N.V.
Francis Wellesplein 1
2018 Antwerpen (BE)

(54) **Interleaving and de-interleaving method for digital data, interleaving and de-interleaving devices, and communication system**

(57) A triangular interleaver (INTERLEAVER) contains a triangular shaped matrix (MAT) of memory cells, each row of which constitutes a first-in-first-out queue. To increase or decrease the interleave depth of the interleaver (INTERLEAVER), the number of interleaved data bytes read from each row of the matrix (MAT) is positively or negatively linearly related to the ordinate number (0, 1, 2, 3, 4) of this row. In this way, impulse noise immunity of transmission of the outgoing interleaved data stream (OID) over a transmission line (TL) is kept substantially independent from transmit rate changes.

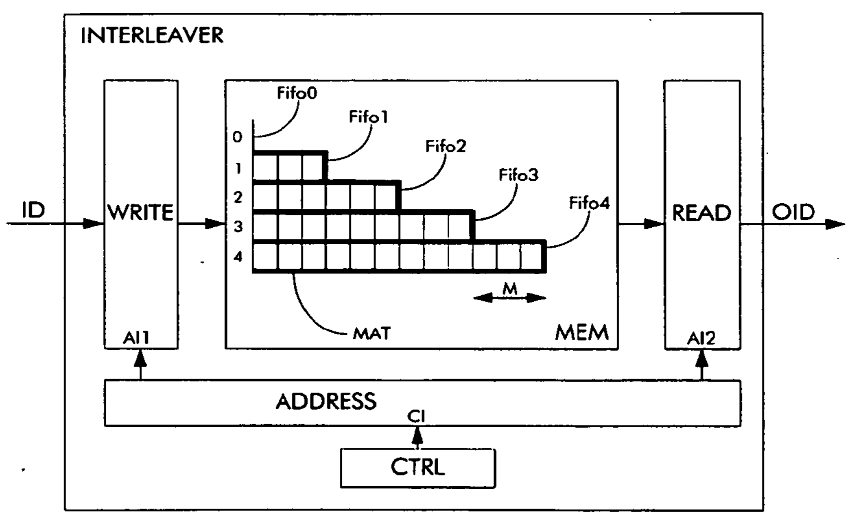

Fig. 2

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Description

The present invention relates to a method for interleaving an incoming data stream as defined in the non-characteristic part of claim 1, a method for de-interleaving an incoming interleaved data stream as defined in the non-characteristic part of claim 11, interleaving and de-interleaving devices as defined in the non-characteristic parts of claim 12 and claim 15 respectively, and a communication system as defined in the non-characteristic part of claim 18.

Such a method for interleaving and de-interleaving, such interleaving and de-interleaving devices and such a communication system are already known in the art, e.g. from the *United States Patent US 4,559,625 entitled 'Interleavers for digital communications' from the inventors Elwyn A. Berlekamp and Po Tong.*

In the communication system described in US 4,559,625, an encoding apparatus develops redundant information in a mathematically prescribed manner and adds this redundant information to the data bytes of codewords. The data bytes of several independently encoded codewords then are re-sequenced by an interleaver. In this way, transmission of the codewords over a transmission link becomes more immune for burst noise of long duration. By re-sequencing the data symbols, burst errors are more evenly distributed over independently encoded codewords. As a consequence, error correction through decoding the transmitted codewords is enhanced. Summarising, the interleaver alters the sequence of data bytes of several codewords to more uniformly distribute the effect of signal degradation or noise on the transmission line over different codewords. In the interleaver, data bytes thereto are entered in memory cells and later on are read out of these memory cells in an order different from the order wherein they entered the memory. The interleaving delay of a data byte is the time interval elapsed between entering and leaving the memory, and usually is expressed as the amount of bytes read out of the memory between the entering and leaving time of the considered data byte. Another important parameter, equal to the number of data bytes in the outgoing interleaved data stream between two data bytes of one and the same codeword, is called the interleaving depth. The interleaving depth is a quantitative indicator of the enhancement of immunity of the transmission for burst noise or the like. In the interleaver described in US 4,559,625, the memory cells wherein data bytes are stored constitute a triangular shaped matrix, i.e. the upper right triangle in the rectangular matrix drawn in Fig. 4a of US 4,559,625. When each row of the triangular shaped matrix is implemented by a first-in-first-out queue, and if incoming data bytes are stored in tail memory cells of the rows while outgoing data bytes are read out of head memory cells of the rows, the interleaving delay of any byte varies linearly related to the ordinal position of the data byte. This is expressed in Col. 2, ln. 34-41 of the cited US Patent. In other words, the interleaving delay of a data byte and the ordinate of the row wherein the data byte is stored are linearly interrelated in the known triangular interleaver. The interleaving depth, which defines the noise immunity of the transmission, is constant and determined by the delay increment per row of the matrix. This delay increment is the difference in length between two successive rows of the matrix, expressed as an amount of memory cells.

In a communication system with variable transmit rates, the effect of interleaving on noise immunity of the transmission depends upon the actual transmit rate. If for instance the transmit rate in a first situation is half the transmit rate in a second situation, burst errors of equal duration will damage in the second situation twice the amount of data bytes damaged in the first situation. If the interleaving depth in situation 2 equals that of situation 1, and the error correction codes added to the codewords are the same in both situations, noise immunity in situation 2 expressed as the maximum duration of a burst error which can be rectified, is only half the noise immunity of situation 1. Communication system designers usually have to realise a certain minimum level of erasure correction to accord with standard specifications. The interleaving depth and error correction code length are chosen by the designer to meet this minimum erasure correction level in a worst case scenario. In a communication system with variable transmit rates, this worst case scenario is the situation wherein data are transmitted at the highest allowable transmit rate. If the above described known interleaver is used and data are transmitted at a lower transmit rate, the noise immunity will be better than required, but this is paid by an interleaving delay which is longer than necessary for an exact adjustment of the noise immunity to the minimum required level at this lower transmit rate.

In other communication systems, it may be wished to have an adaptable noise immunity so that the capacity for restoring the effect of burst noise errors on the transmission line may be modified in function of the quality of the line, the noise pollution, service dependent or user dependent requirements, and so on.

It is therefore an object of the present invention to provide a method for interleaving and de-interleaving, interleaving and de-interleaving devices and a communication system of the known type, but wherein noise immunity can be modified or can be made independent from the transmit rate over the transmission line.

According to the invention, this object is realised by the method for interleaving an incoming data stream defined in claim 1, the method for de-interleaving an interleaved data stream defined in claim 11, the interleaving and de-interleaving devices defined in claims 12 and 15 respectively, and the communication system defined in claim 18.

An obvious way to realise the above described object is to adapt the shape of the triangular matrix by emptying the interleaving memory completely and re-

formatting the triangular shaped matrix so that for instance the delay increment per row of the matrix increases. By adapting for instance the delay increment per row each time the transmit rate changes, the interleaving depth changes accordingly as a result of which the noise immunity remains substantially independent from the transmit rate. This obvious way however is not very efficient because it involves a very long transition state, wherein transmission has to be interrupted.

According to the invention, the interleave depth is modified by adapting the shape of the triangular array in a dynamic way, i.e. without emptying the whole interleaving memory. Indeed, if the number of interleaved data bytes read from a row of the matrix is linearly related to the ordinate of this row, the delay increment per row of the matrix is decreased or increased. If for instance 1 data byte is read from row 1, two data bytes are read from row 2, ..., I-1 data bytes are read from row I-1, the difference in length between two successive rows of the matrix (which is the delay increment per row) is decreased by 1.

It is to be noticed that the term 'comprising', used in the claims, should not be interpreted as being imitative to the means listed thereafter. Thus, the scope of the expression 'a device comprising means A and B' should not be limited to devices consisting only of components A and B. It means that with respect to the present invention, the only relevant components of the device are A and B.

Similarly, it is to be noted that the term 'coupled', also used in the claims should not be interpreted as being limitative to direct connections only. Thus, the scope of the expression 'a means A coupled to a means B' should not be limited to devices or systems wherein an output of means A is directly connected to an input of means B. It just means that there exists a path between an output of A and an input of B which may be a path including other devices or means.

Another remark is that an obvious variant of the present system and method is one wherein the role of columns and rows of the interleaving or de-interleaving matrix is inverted. Applicability of the present invention clearly is not restricted to those implementations wherein rows of the matrices are drawn horizontally and columns are drawn vertically. For evident reasons, one obtains the same technical result when the terms 'column' and 'row' are interchanged throughout the whole application. The scope of protection defined by the claim hence should also not be limited to embodiments of the present invention wherein 'row' is synonymous for a horizontal structure and 'column' is per se associated with a vertical structure.

Furthermore, it should be stressed that the ordinate numbers of rows or columns in the interleaving and/or de-interleaving matrices may be increasing from bottom to top, from top to bottom, from left to right or from right to left according to the designers preferences. As a consequence, the triangular shaped matrix may have a top pointing in upward, downward, left or right directions. For the designer it is only important to have an addressing conform to his/her choice of ordinate numbers. The scope of the claims should not be interpreted as being limitative for this choice.

A further feature of the present method for interleaving is defined in claim 2.

In this way, a less complex interleaver can be realised since the amount of outgoing interleaved data bytes read from a row of the matrix then becomes independent from the amount of data bytes written in this row.

An additional characteristic feature of the present invention is defined in claim 3.

In this way, the noise immunity is kept constant in a system with variable transmit rates.

It is remarked here that the delay increment per row of the interleaving triangular matrix may also be adapted according to the present invention in systems with constant transmit rates to increase or decrease the error protection therein. As already suggested above, other criteria than the increase or decrease of the transmit rate have to be used in such systems to decide when bytes are read out of the matrix according to the present invention. If in such a system the delay increment per row increases, the interleaving depth increases accordingly as a consequence of which the error protection has improved. Similarly, the error protection becomes worse when the delay increment per row is decreased.

Yet another feature of the present method is defined in claim 4.

Thus, when the transmit rate on the transmission line remains substantially constant, data bytes are written in and read out of the triangular shaped matrix in the known manner.

Another feature of the present method is defined in claim 5.

Indeed, if the rows of the triangular matrix are numbered so that the ordinate numbers grow with the length of the row, the delay increment per row decreases when the number of read interleaved data bytes per row is positively related to the ordinate number of the row. A decreased delay increment per row results in a decreased interleaving depth and hence in a lower burst noise immunity. The decrease of the transmit rate on the other hand has an increasing effect on the burst noise immunity. Both effects may compensate so that the noise immunity remains substantially independent from the transmit rate.

Yet another feature of the present method is defined in claim 6.

Indeed, if the rows of the triangular shaped matrix are again numbered so that the ordinate numbers grow with the length of the rows, it can be deduced in a similar way as above that the noise immunity remains substantially insensitive for a transmit rate increase if the amount of interleaved data bytes read from the rows of

the matrix is negatively related to the ordinate numbers of these rows.

To decrease the interleave depth, outgoing data bytes may be read as defined in claim 7, in a first particular implementation of the present method.

Indeed, the number of data bytes read from each row in the matrix is equal to the ordinate number of the row. As will be explained later, this implementation requires the presence of a buffer in both the interleaver and de-interleaver.

In a second particular implementation of the present method for interleaving, outgoing data bytes may be read as defined in claim 8 to decrease the interleaving depth.

In this way, the number of data bytes read from each row in the matrix is again equal to the ordinate number of the row. The dummy bytes are inserted at the interleaver but not de-interleaved in the de-interleaver. An advantage of this implementation is that there is no buffer needed at the de-interleaver but the size of the interleavers buffer, as will be shown later, has doubled. Another advantage thereof is that the interleaver and the de-interleaver can be obtained than for the first particular implementation, and the noise immunity stays constant while adapting the interleave depth.

To increase the delay increment per row, a first particular implementation is defined in claim 9 and a second implementation is defined in claim 10.

Similar to the implementations for decreasing the delay increment, defined in claims 7 and 8, the second implementation may be realised in a less complex way and requires no buffer in the interleaver or de-interleaver. The first implementation requires the presence of a buffer in the interleaver but realises a better throughput since no bandwidth is used to transport dummy bytes.

The above and other objects and features of the invention will become more apparent and the invention itself will be best understood by referring to the following description of an embodiment taken in conjunction with the accompanying drawings wherein:

Fig. 1 is a block scheme of an embodiment of the communication system according to the present invention;

Fig. 2 is a block scheme of an embodiment of the interleaving device INTERLEAVER according to the present invention;

Fig. 3 is a block scheme of an embodiment of the de-interleaving device DE-INTERLEAVER according to the present invention;

Fig. 4A is a drawing illustrating the filling of the interleaving memory conform the known method with data bytes during a steady state wherein the delay increment M is 3;

Fig. 4B is a drawing illustrating the filling of the de-interleaving memory conform the known method with data bytes during the steady state wherein the delay increment M is 3;

Fig. 5A is a drawing illustrating the filling of the interleaving memory with data bytes during a transition state wherein the delay increment M is reduced from 3 to 2;

Fig. 5B is a drawing illustrating the filling of the de-interleaving memory with data bytes during this transition state wherein the delay increment M is reduced from 3 to 2;

Fig. 6A is a drawing illustrating the filling of the interleaving memory with data bytes during a transition state wherein the delay increment M is in creased from 3 to 4; and

Fig. 6B is a drawing illustrating the filling of the de-interleaving memory with data bytes during this transition state wherein the delay increment M is increased from 3 to 4.

The communication system drawn in Fig. 1 consists of a transmitter TX, a receiver RX and a transmission line TL. The transmitter TX includes a data source DATA SOURCE, an encoder ENCODER, an interleaving device INTERLEAVER and a modulator MOD. The receiver RX includes a demodulator DMOD, a de-interleaving device DE-INTERLEAVER, a decoder DECODER and a data sink DATA SINK.

An output of the transmitter TX is coupled to an input of the receiver RX via the transmission line TL. Inside the transmitter TX, the data source DATA SOURCE, the encoder ENCODER, the interleaver INTERLEAVER and the modulator MOD are cascade connected. An output of the modulator MOD is coupled to the transmission line TL via the transmitter output. The other end of the transmission line TL is coupled to an input of the demodulator DMOD via the receiver input. Inside the receiver RX, the demodulator DMOD, the de-interleaver DE-INTERLEAVER, the decoder DECODER and the data sink DATA SINK are cascade connected.

The data source DATA SOURCE produces a data stream which may comprise user data bytes and/or overhead data bytes. A fixed amount of these bytes constitutes a single word and each one of these words is encoded by the encoder ENCODER. This implies that the encoder ENCODER extends each of the words according to predefined mathematical schemes by adding redundant bytes thereto. These redundant bytes and the mathematical schemes will enable the receiver RX to detect and probably to correct errors in transmitted words. The extended words generated by the encoder ENCODER are called codewords and constitute an incoming data stream ID for the interleaver INTERLEAVER. By re-sequencing the data bytes of different codewords of the incoming data stream ID, the interleaver INTERLEAVER produces an outgoing interleaved data stream OID which is better protected for burst noise on the transmission line TL than the incoming data stream ID. The modulator MOD finally modu-

lates data symbols, i.e. combinations of data bits of the data stream OID which represent one point in the constellation scheme of the modulation method, on one or more carriers to be transmitted over the transmission line TL.

At the receiver RX, the demodulator DMOD demodulates the data symbols from the carrier(s) and generates from the demodulated data symbols a stream of data bytes named the incoming interleaved data stream IID. The bytes of the incoming interleaved data stream IID are re-sequenced in the de-interleaver DE-INTERLEAVER so that the effect of the interleaver INTERLEAVER on the order of bytes is compensated for and the generated outgoing data stream OD again contains the original sequence of data bytes. In the decoder DECODER, errors due to transmission are detected and corrected by using the already mentioned mathematical schemes and the information of the redundantly added bytes. The so determined data stream then is applied to the data sink DATA SINK, which may be any kind of terminal, interface or the like.

In the communication system of Fig. 1, the interleaver INTERLEAVER and de-interleaver DE-INTERLEAVER are designed to provide to the transmitted data stream a transmit rate independent impulse noise immunity. The INTERLEAVER and DE-INTERLEAVER structure which realise this object, is drawn in Fig. 2 and Fig. 3 respectively, and is described in detail in the following paragraphs.

The interleaver INTERLEAVER of Fig. 2 includes writing means WRITE, reading means READ, a memory MEM, an address generator ADDRESS and a controller CTRL. The memory MEM is equipped with a triangular shaped matrix MAT of memory cells wherein each row is constituted by a first-in-first-out queue of memory cells. In Fig. 2, five rows of the matrix MAT with respective ordinates 0, 1, 2, 3 and 4 are constituted by the queues Fifo0, Fifo1, Fifo2, Fifo3, and Fifo4 which have an incrementally growing length, the increment per row being equal to M=3.

The writing means WRITE, the memory MEM, and the reading means READ are cascade connected between the incoming data input ID and an outgoing interleaved data output OID of the interleaver INTERLEAVER. An output of the controller CTRL and a control input CI of the address generator ADDRESS are interconnected and two outputs of the address generator ADDRESS are coupled to address inputs AI1 of the writing means WRITE and AI2 of the reading means READ respectively.

The incoming data bytes applied to the interleaver INTERLEAVER via its incoming data input ID are written in tail memory cells of the queues of the interleaving matrix MAT. Simultaneously, outgoing data bytes are read out of head memory cells of the queues of the matrix MAT by the reading means READ and applied to the outgoing data output OID of the interleaver INTERLEAVER. In which queue the writing means WRITE has to store incoming data bytes and from which memory cells the reading means READ has to read outgoing data bytes is defined by the addresses generated by the address generator ADDRESS. Indeed, address generator ADDRESS generates a first sequence of row ordinates or write addresses indicating to which rows of the interleaving matrix MAT subsequent incoming data bytes are to be applied and a second sequence of row ordinates or read addresses indicating from which rows of the interleaving matrix MAT subsequent outgoing data symbols are to be read. How both sequences look like depends upon the state wherein the address generator ADDRESS is set by the controller CTRL. The following paragraphs briefly describe three states wherein the address generator ADDRESS can be set.

If the address generator ADDRESS is set in a steady state, subsequent incoming data bytes are applied to subsequent rows of the matrix MAT in a circular way. With reference to Fig. 2, this means that a first incoming data byte is applied to Fifo0, a second is applied to Fifo1, a third is applied to Fifo2, a fourth is applied to Fifo3, a fifth is applied to Fifo4, a sixth is again applied to Fifo0 and so on. Subsequent outgoing data bytes are, still during this steady state, read from subsequent rows of the matrix MAT in a circular way. This is realised for instance if the incoming and outgoing rates are equal and a byte is read from each row wherein a byte is written. Since the rows have different lengths, subsequently read data bytes were not subsequently written in the matrix MAT.

If the address generator ADDRESS is set in a transition state during which the interleaving depth is decreased, the number of data bytes read from each row of the matrix MAT is positively linearly related to the ordinate of that row. At the end of this transition state, the increment parameter M is decreased and also the average interleaving delay (the time between entering and leaving the interleaver INTERLEAVER for a single data byte) is decreased.

If the address generator ADDRESS is set in a transition state during which the interleaving depth is increased, the number of data bytes read from each row of the matrix MAT is negatively linearly related to the ordinate of that row. At the end of this transition state, the increment parameter M is increased and also the average interleaving delay is increased.

Summarising, the sequence of reading data bytes from the interleaver INTERLEAVER differs in different states. More details concerning this will be given later. First, the structure of the de-interleaver DE-INTERLEAVER drawn in Fig. 3 is described.

The de-interleaver DE-INTERLEAVER of Fig. 3 includes writing means WRITE', reading means READ', a memory MEM', an address generator ADDRESS' and a controller CTRL'. The memory MEM' is equipped with a triangular shaped matrix MAT' of memory cells wherein each row is constituted by a first-in-first-out queue of memory cells. In Fig. 3, five rows of the matrix

MAT' with respective ordinates 0, 1, 2, 3 and 4 are constituted by the queues Fifo0', Fifo1', Fifo2', Fifo3' and Fifo4' which have a decrementally shrinking length, the decrement per row being M=3.

The writing means WRITE', the memory means MEM', and the reading means READ' are cascade connected between the incoming interleaved data input IID and the outgoing data output OD of the de-interleaver DE-INTERLEAVER. An output of the controller CTRL' and a control input CI' of the address generator ADDRESS' are interconnected and two outputs of the address generator ADDRESS' are coupled to address inputs AI1' of the writing means WRITE' and AI2' of the reading means READ' respectively.

The incoming interleaved data bytes applied to the de-interleaver DE-INTERLEAVER via its incoming interleaved data input IID are written in tail memory cells of the queues of the de-interleaving matrix MAT'. Meanwhile, outgoing data bytes are read out of head memory cells of the queues of the matrix MAT' by the reading means READ' and applied to the outgoing data output OD of the de-interleaver DE-INTERLEAVER. In which memory cells the writing means WRITE' has to write data bytes and from which memory cells the reading means READ' has to deduce data bytes is defined by the addresses generated by the address generator ADDRESS'. This address generator ADDRESS' generates a first sequence of row ordinates or write addresses indicating to which rows of the interleaving matrix MAT' subsequent incoming interleaved data bytes are to be applied, and a second sequence of row ordinates or read addresses indicating from which rows of the interleaving matrix MAT' subsequent outgoing data bytes are to be read. How both sequences look like depends upon the state wherein the address generator ADDRESS' is set by the controller CTRL'. The following paragraphs again briefly describe three states wherein the address generator ADDRESS' can be set.

If the address generator ADDRESS' is set in a steady state, subsequent incoming interleaved data bytes are applied to subsequent rows of the matrix MAT', and subsequent outgoing data bytes are read from subsequent rows of the matrix MAT' in a circular way. Thus, each time an incoming byte is written in the head memory cell of a queue, an outgoing byte is read from this queue. Since the sum of the length of a queue in the interleaver INTERLEAVER of Fig. 2 and the length of the corresponding queue in the de-interleaver DE-INTERLEAVER of Fig. 3 is constant, the global interleaving/de-interleaving delay is the same for all bytes.

If the address generator ADDRESS' is set in a transition state during which the interleave depth is decreased, the number of data bytes written in each row of the matrix MAT' is positively linearly related to the ordinate of that row. At the end of this transition state, the decrement parameter M is decreased and also the average de-interleaving delay (the time between entering and leaving the de-interleaver DE-INTERLEAVER) is decreased.

If the address generator ADDRESS' is set in a transition state during which the interleave depth is increased, the number of data bytes written in each row of the matrix MAT' is negatively linearly related to the ordinate of that row. At the end of this transition state, the decrement parameter M is increased and also the average de-interleaving delay is increased.

Summarising, the sequence of writing data bytes in the de-interleaver DE-INTERLEAVER differs for different states. More details concerning this are given in the next paragraphs.

The filling of the interleaving and de-interleaving matrices MAT and MAT' in the above defined states will be described more detailed now. First, referring to Fig. 4A and Fig. 4B, the filling of the matrices MAT and MAT' will be described when the address generators, ADDRESS and ADDRESS', operate in the steady state wherein the delay increment parameter M equals 3. Secondly, it is assumed that the address generators, ADDRESS and ADDRESS', are brought into the transition state wherein the delay increment parameter M is reduced from 3 to 2. Reference will be made to Fig. 5A and Fig. 5B when explaining the filling of MAT and MAT' in this state. In a last paragraph, the address generators, ADDRESS and ADDRESS', are set in the transition state wherein the delay increment parameter M is increased from 3 to 4. The filling of MAT and MAT' during this last state is described by referring to Fig. 6A and Fig. 6B.

In Fig. 4A, the matrix MAT is shown. Each row of this matrix MAT is constituted by a first-in-first-out memory, with tail memory cell at the leftmost side and head memory cell at the rightmost side. If a byte is applied to a row of matrix MAT, it is thus stored in the tail memory cell. Before writing this byte in the tail memory cell however, the byte contained by the head memory cell is read and all bytes in the first-in-first-out memory are shifted one position towards the head memory cell. Such a first-in-first-out memory may be realised in hardware (e.g. a shift register) or software (by adapting the tail and head memory cell pointers with a program each time a byte is written or read). The write-to-read delay experienced by a byte applied to a row of the matrix MAT is proportional to the length of the first-in-first-out memory constituting that row. The matrix drawn in Fig. 4A contains 5 rows with ordinates 0, 1, 2, 3 and 4 and first-in-first-out memories Fifo0, Fifo1, Fifo2, Fifo3 and Fifo4. The delay experienced by a byte in MAT is equal to j.M.I. Herein, j represents the ordinate of the row, M represents the delay increment per row, and I represents the number of rows in the matrix MAT.

The de-interleaving matrix MAT' of Fig. 4B is similar to the interleaving matrix MAT of Fig. 4A but the row ordinates are reversed so that row ordinates corresponding to short first-in-first-out memories in the interleaving matrix MAT, correspond to long first-in-first-out

memories in the de-interleaving matrix MAT'.

When a byte is applied to a row, for instance row 2, in the interleaver INTERLEAVER, it is stored in the tail memory cell of Fifo2 after a byte is read from the head memory cell of Fifo2 to be transmitted over the transmission line TL of Fig. 1. Upon receipt by the de-interleaver DE-INTERLEAVER, this byte is stored in the tail memory cell of Fifo2' after a byte is read from the head memory cell of Fifo2'. Since the sum of the write-to-read delay of a row of the interleaver INTERLEAVER and that of the corresponding row of the de-interleaver DE-INTERLEAVER is constant, each byte experiences the same global delay. Subsequent incoming bytes are written in subsequent rows of the matrix MAT. The first byte experiences no interleaving delay and is immediately transmitted to the receiver. Fifo0 therefore is an empty queue in Fig. 4A. The second byte is written in Fifo1 which is indicated by w2 in Fig. 4A. The third byte, fourth byte and fifth byte are applied to Fifo2, Fifo3 and Fifo4 respectively and fill the memory cells marked by w3, w4 and w5. The sixth byte again passes through Fifo0 and experiences no interleaving delay and bytes 7, 8, 9 and 10 are subsequently stored in the new tail memory cells of Fifo1, Fifo2, Fifo3 and Fifo4 marked by w7, w8, w9 and w10 respectively. While writing bytes in the tail memory cells of the queues, bytes are read from the head memory cells. Hence the first byte is transmitted without interleaving delay, and is followed by bytes r2, r3, r4, r5 read from Fifo1, Fifo2, Fifo3 and Fifo4 respectively. Then, again a byte is transmitted without interleaving delay and this one is followed by bytes r7, r8, r9 and r10. The indexes used in Fig. 4B with prefixes w and r in a similar way indicate how the interleaved incoming stream of bytes is stored in the de-interleaving matrix MAT' and read therefrom to constitute the non-interleaved output data stream. In Fig. 4B, Fifo4' is an empty queue which indicates that bytes applied to this row experience no de-interleaving delay.

During the steady state of the system, the different bitrates at inputs and outputs of the interleaver and de-interleaver are supposed to be equal. The interleaving depth D is equal to I*M+1. Herein, I again represents the number of rows in the interleaving matrix MAT.

The transition state wherein M is decreased from 3 to 2 is entered by writing a byte w1 in a memory cell of Fifo0. Instead of reading a byte from Fifo0, a byte r1 is read now from Fifo4 now. The next bytes to be transmitted are read from :

- Fifo3 (r2) and Fifo4 (r3);
- Fifo2 (r4), Fifo3 (r5) and Fifo4 (r6);
- Fifo1 (r7), Fifo2 (r8), Fifo3 (r9) and Fifo4 (r10).

Meanwhile, the bytes w2 to w10 are written in the memory of the interleaver. The bytes that are read from the matrix MAT in the interleaver are transmitted towards the receiver and stored in the de-interleaver in corresponding rows of the matrix MAT'. The bytes r1 to r10 of Fig. 5A thus represent bytes w1' to w10' in Fig. 5B. Similarly, bytes r1' to r10' are read from the matrix MAT' to constitute the de-interleaved output data stream that is applied to the decoder of Fig. 1. The bytes that are written and read during the transition state are shaded grey in Fig. 5A and Fig. 5B. At the end of the transition state, a buffer BUF of size I.(I-1)/2 is present in both the interleaver (see Fig. 5A) and de-interleaver (see Fig. 5B). To obtain an interleaver with delay increment parameter M=2, these 2 buffers BUF have to be emptied. The memory requirement for performing the transition from M=3 to M=2 is thus I(I-1)/2 bytes in the interleaver and in the de-interleaver. This memory may be provided by an enlarged capacity of the first-in-first-out queues of the matrices MAT and MAT', or can be implemented by a normal memory without a first-in-first-out structure.

It is to be remarked that instead of transmitting only useful bytes over the transmission line TL, dummy bytes can be inserted in the transmitted data stream. Such dummy bytes are not de-interleaved. An alternative transmission sequence for the one described above is as follows:

- 4 dummy bytes are transmitted, byte r1 from Fifo4 is transmitted;
- 3 dummy bytes are transmitted, bytes r2 and r3 from Fifo3 and Fifo4 are transmitted;
- 2 dummy bytes are transmitted, bytes r4, r5 and r6 from Fifo2, Fifo3 and Fifo4 are transmitted;
- 1 dummy byte is transmitted, bytes r7, r8, r9 and r10 from Fifo 1, Fifo2, Fifo3 and Fifo4 are transmitted.

Compared to the above version of the transition state, the latter implementation has the drawback of using part of the bandwidth on the transmission line TL for transmission of dummy bytes but has the advantage of not losing immunity during the modification of M. The latter implementation moreover requires no buffer BUF in the de-interleaver but the size of the interleaver buffer has doubled.

If the transmit rate for transmission over the line TL increases, the interleave depth D also has to increase to keep constant impulse noise immunity. This can again be realised by manipulating M and the structure of the matrices MAT and MAT'. The following paragraphs will clarify how M can be increased from 3 to 4 during the transition state illustrated by Fig. 6A and Fig. 6B.

The transition phase to increase M from 3 to 4 is initiated by filling a buffer BUF of I.(I-1) bytes in the interleaver. Afterwards, following sequence of bytes is transmitted:

- a byte (r1) from Fifo0;
- a byte (r2) from Fifo0 and a byte (r3) from Fifo1;
- a byte (r4) from Fifo0, a byte (r5) from Fifo1 and a byte (r6) from Fifo2;
- a byte (r7) from Fifo0, a byte (r8) from Fifo1, a byte

(r9) from Fifo2 and a byte (r10) from Fifo3.

During this transition state, bytes transmitted over the transmission line TL are written in the corresponding rows of the de-interleaver memory but no bytes are read from the de-interleaver memory. The de-interleaver and interleaver return to the steady state with delay increment M=4 after the transition state. In the interleaver memory, a buffer BUF of I.(I-1)/2 memory cells contains bytes now. To obtain an interleaver with delay increment M=4, this buffer BUF has to be emptied. The memory requirement for performing the transition from M=3 to M=4 is I.(I-1) bytes in the interleaver. This may again be provided by an enlarged capacity of the first-in-first-out memories Fifo0, Fifo1, Fifo2, Fifo3 and Fifo4 of the matrix MAT, or the buffer BUF can be implemented by a normal memory without first-in-first-out structure.

It is to be remarked that instead of transmitting only useful bytes over the transmission line TL, one can again think of an alternative implementation wherein dummy bytes are transmitted. The sequence for transmitting bytes may then be as follows:

- a byte (r1) from Fifo0 followed by 4 dummy bytes;
- a byte (r2) from Fifo0 and a byte (r2) from Fifo1 followed by 3 dummy bytes;
- a byte (r4) from Fifo0, a byte (r5) from Fifo1 and a byte (r6) from Fifo2 followed by 2 dummy bytes; and
- a byte (r7) from Fifo0, a byte (r8) from Fifo1, a byte (r9) from Fifo2 and a byte (r10) from Fifo3, followed by a dummy byte.

Compared to the first version, the latter implementation of the transition state again has the drawback of using part of the bandwidth on the transmission line TL for transmission of dummy bytes but has the advantage of not losing immunity during the modification of M. The latter implementation moreover requires no buffer in the interleaver, and the address generator may be less complex.

It is to be noted that the applicability of the present invention is not restricted by the transmission medium of the transmission line TL. In particular, any connection between the transmitter TX and receiver RX, e.g. a cable connection, a telephone line, a satellite connection, an optical fibre, a radio link through the air, and so on may be affected by burst noise and can thus be protected by a method according to the present invention.

The present invention is very suitable for being used in VSDL (Very High Speed Digital Subscriber Line) modems or the like. These modems will transport digital data at high bitrates over telephone lines. The telephone lines may be affected by several sources of burst noise, especially when the lines are stretched through the air. Radio interference from radio amateurs, critical weather conditions, transient appearances due to ringing and hooking are a few of the noise sources affecting transmission over such telephone lines. Although the present invention is an attractive solution for providing transmit rate independent impulse noise immunity in such VSDL systems, the applicability of the present invention is not limited to these systems or to similar systems having the same type of modulation and/or encoding. As will be recognised by a person skilled in the art, the modulation constellation and encoding scheme used by the modulator and the encoder respectively are of no importance for the present invention.

It is further remarked that the transmitter TX and receiver RX according to the present invention may be integrated in a single transceiver. This is so in modems which are adapted to transmit and receive data to and from a bi-directional transmission line. In case the transmitter and receiver are integrated, the triangular interleaving and de-interleaving matrixes, MAT and MAT', may be grouped to constitute a rectangular interleaving/de-interleaving matrix. Obviously, also the functionality of both writing means, WRITE and WRITE', both reading means, READ and READ', both addressing means, ADDRESS and ADDRESS', and both controllers, CTRL and CTRL', may be combined and integrated in one writing unit, one reading unit, one addressing unit and one control unit respectively.

Furthermore it is noticed that via the present invention, the delay increment parameter M may be increased or decreased by more than one unit. As well for the decreasing as for the increasing process, it suffices to execute the above described transition states more than once.

While the principles of the invention have been described above in connection with specific apparatus, it is to be clearly understood that this description is made only by way of example and not as a limitation on the scope of the invention.

Claims

1. Method for interleaving incoming data bytes (w1, ..., w10) of an incoming data stream (ID) to thereby generate an outgoing interleaved data stream (OID) of outgoing interleaved data bytes (r1, ..., r10), wherein said incoming data bytes (w1, ..., w10) are written in tail memory cells of rows of a triangular shaped matrix (MAT) of memory cells, each row of memory cells in said matrix (MAT) representing a first-in-first-out queue (Fifo0, Fifo1, Fifo2, Fifo3, Fifo4), and wherein said outgoing interleaved data bytes (r1, ..., r10) are read from head memory cells of said rows thereby realising said outgoing interleaved data stream (OID),

   CHARACTERISED IN THAT from each row an amount of said outgoing interleaved data bytes (r1, ..., r10) is read which is nearly related to an ordinate number (0, 1, 2, 3, 4) of said row in said triangular shaped matrix (MAT).

2. Method for interleaving according to claim 1, **CHARACTERISED IN THAT** meanwhile in each row of said triangular shaped matrix (MAT) an equal amount of said incoming data bytes (w1, ..., w10) is written.

3. Method for interleaving according to claim 1, **CHARACTERISED IN THAT** reading said outgoing interleaved data bytes (r1, ..., r10) is performed this way when the transmit rate for transmission of said outgoing interleaved data stream (OID) over a transmission line (TL) increases or decreases.

4. Method for interleaving according to claim 3, **CHARACTERISED IN THAT** when said transmit rate remains substantially constant, an equal amount of said incoming data bytes (w1, ..., w10) is written in each row of said triangular shaped matrix (MAT) while an equal amount of said outgoing interleaved data bytes (r1, ..., r10) is read from each row.

5. Method for interleaving according to claim 3, **CHARACTERISED IN THAT** when said transmit rate decreases, said amount of said outgoing interleaved data bytes (r1, ..., r10) read is positively related to said ordinate number (0, 1, 2, 3, 4).

6. Method for interleaving according to claim 3, **CHARACTERISED IN THAT** when said transmit rate increases, said amount of said outgoing interleaved data bytes (r1, ..., r10) read is negatively related to said ordinate number (0, 1, 2, 3, 4).

7. Method for interleaving according to claim 5, **CHARACTERISED IN THAT** when said transmit rate decreases, successive outgoing interleaved data bytes (r1, ..., r10) are read from:

- row I;
- row I-1 and row I;
- row I-2, row I-1 and row I,

and so on until outgoing interleaved data bytes are read from row 1 to row I-1, I being the number of rows in said triangular shaped matrix (MAT).

8. Method for interleaving according to claim 7, **CHARACTERISED IN THAT**

I-1 dummy bytes are generated and inserted in said outgoing interleaved data stream (OID) before a first outgoing interleaved data byte is read out of row I;
I-2 dummy bytes are generated and inserted in said outgoing interleaved data stream (OID) before a first outgoing interleaved data byte is read out of row I-1;
I-3 dummy bytes are generated and inserted in said outgoing interleaved data stream (OID) before a first outgoing interleaved data byte is read out of row I-2,

and so on.

9. Method for interleaving according to claim 6, **CHARACTERISED IN THAT** when said transmit rate increases, successive outgoing interleaved data bytes (r1, ..., r10) are read from:

- row 0;
- row 0 and row 1;
- row 0, row 1 and row 2,

and so on until outgoing interleaved data bytes are read from row 0 to row I-2, I being the number of rows in said triangular shaped matrix (MAT).

10. Method for interleaving according to claim 9, **CHARACTERISED IN THAT**

I-1 dummy bytes are generated and inserted in said outgoing interleaved data stream (OID) after a first outgoing interleaved data byte is read out of row 0;
I-2 dummy bytes are generated and inserted in said outgoing interleaved data stream (OID) after a first outgoing interleaved data byte is read out of row 1;
I-3 dummy bytes are generated and inserted in said outgoing interleaved data stream (OID) after a first outgoing interleaved data byte is read out of row 2,

and so on.

11. Method for de-interleaving incoming interleaved data bytes (w1', ..., w10') of an incoming interleaved data stream (IID) to thereby generate an outgoing data stream (OD) of outgoing data bytes (r1', ..., r10'), wherein said incoming interleaved data bytes (w1', ..., w10') are written in tail memory cells of rows of a triangular shaped matrix (MAT') of memory cells, each row of memory cells in said matrix (MAT) representing a first-in-first-out queue (Fifo0', Fifo1', Fifo2', Fifo3', Fifo4'), and wherein said outgoing data bytes (r1', ..., r10') are read from head memory cells of said rows thereby realising said outgoing data stream (OD),
CHARACTERISED IN THAT in each row of said triangular shaped matrix (MAT') an amount of said incoming interleaved data bytes (w1', ..., w10') is written which is linearly related to an ordinate

number (0, 1, 2, 3, 4) of said row in said triangular shaped matrix (MAT').

12. Interleaving device (INTERLEAVER) used to re-sequence incoming data bytes (w1, ..., w10) of an incoming data stream (ID) to thereby generate an outgoing interleaved data stream (OID) of outgoing interleaved data bytes (r1, ..., r10), said interleaving device (INTERLEAVER) comprising:

a. memory means (MEM) including a plurality of first- in- first-out queues (Fifo0, Fifo1, Fifo2, Fifo3, Fifo4) adapted to represent respective rows of a triangular shaped matrix (MAT) of memory cells;
b. writing means (WRITE) with an output coupled to an input of said memory means (MEM), said writing means (WRITE) being adapted to write each one of said incoming data bytes (w1, ..., w10) in a tail memory cell of one of said rows identified by a write address;
c. reading means (READ) with an input coupled to an output of said memory means (MEM), said reading means (READ) being adapted to read each one of said outgoing interleaved data bytes (r1, ..., r10) from a head memory cell of one of said rows identified by a read address; and
d. address generating means (ADDRESS), a first output of which is coupled to an address input (AI1) of said writing means (WRITE) and a second output of which is coupled to an address input (AI2) of said reading means (READ), said address generating means (ADDRESS) being adapted to generate said write address and said read address,

CHARACTERISED IN THAT said address generating means (ADDRESS) is further adapted to generate for each row an amount of read addresses which is linearly related to an ordinate number (0, 1, 2, 3, 4) of said row in said triangular shaped matrix (MAT).

13. Interleaving device (INTERLEAVER) according to claim 12,
CHARACTERISED IN THAT said interleaving device (INTERLEAVER) further includes:

e. control means (CTRL), an output of which is coupled to a control input (CI) of said address generating means (ADDRESS), said control means (CTRL) being adapted to bring said address generating means (ADDRESS) either in a steady state or a transition state; and further in that
f. said address generating means (ADDRESS) is adapted to generate said read addresses in this way in said transition state, and is adapted to generate, in said steady state, for each row of said triangular shaped matrix (MAT) an equal amount of read addresses, and meanwhile to generate for each row an equal amount of write addresses.

14. Interleaving device (INTERLEAVER) according to claim 12,
CHARACTERISED IN THAT said memory means (MEM) further is provided with:

g. a buffer of at most I*(I-1) memory cells, I being the number of rows in said triangular shaped matrix (MAT), said buffer being adapted to temporarily store part of said incoming data bytes (w1, ..., w10).

15. De-interleaving device (DE-INTERLEAVER) used to re-sequence incoming interleaved data bytes (w1', ..., w10') of an incoming interleaved data stream (IID) to thereby generate an outgoing data stream (OD) of outgoing data bytes (r1', ..., r10'), said de-interleaving device (DE-INTERLEAVER) comprising :

a. memory means (MEM') including a plurality of first-in-first-out queues (Fifo0', Fifo1', Fifo2', Fifo3', Fifo4') adapted to represent respective rows of a triangular shaped matrix (MAT') of memory cells;
b. writing means (WRITE') with an output coupled to an input of said memory means (MEM'), said writing means (WRITE') being adapted to write each one of said incoming interleaved data bytes (w1', ..., w10') in a tail memory cell of one of said rows identified by a write address;
c. reading means (READ') with an input coupled to an output of said memory means (MEM'), said reading means (READ') being adapted to read each one of said outgoing data bytes (r1', ..., r10') from a head memory cell of one of said rows identified by a read address; and
d. address generating means (ADDRESS'), a first output of which is coupled to an address input (AI1') of said writing means (WRITE') and a second output of which is coupled to an address input (AI2') of said reading means (READ'), said address generating means (ADDRESS') being adapted to generate said write address and said read address,

CHARACTERISED IN THAT said address generating means (ADDRESS') further is adapted to generate for each row of said triangular shaped matrix (MAT') an amount of write addresses which

is linearly related to an ordinate number (0, 1, 2, 3, 4) of said row in said triangular shaped matrix (MAT').

16. De-interleaving device (DE-INTERLEAVER) according to claim 15,

CHARACTERISED IN THAT said de-interleaving device (DE-INTERLEAVER) further includes:

e. control means (CTRL'), an output of which is coupled to a control input (CI') of said address generating means (ADDRESS'), said control means (CTRL') being adapted to bring said address generating means (ADDRESS') either in a steady state or a transition state; and further in that

f. said address generating means (ADDRESS') is adapted to generate said write addresses in this way in said transition state, and is adapted to generate, in said steady state, for each row of said triangular shaped matrix (MAT') an equal amount of read addresses, and meanwhile to generate for each row an equal amount of write addresses.

17. De-interleaving device (DE-INTERLEAVER) according to claim 15,

CHARACTERISED IN THAT said memory means (MEM') further is provided with:

g. a buffer of at most I*(I-1)/2 memory cells, I being the number of rows in said triangular shaped matrix (MAT'), said buffer being adapted to temporarily store part of said incoming interleaved data bytes (w1', ..., w10').

18. A communication system comprising a transmitter (TX) coupled via a transmission line (TL) to a receiver (RX), said transmitter (TX) comprising the cascade connection of:

a. a data source (DATA SOURCE) provided to generate a data stream;

b. encoding means (ENCODER) provided to extend words of said data stream with redundant information to thereby generate codewords of an incoming data stream (ID);

c. interleaving means (INTERLEAVER) provided to re-sequence incoming data bytes (w1, ..., w10) of said incoming data stream (ID) to thereby generate an outgoing interleaved data stream (OID) of outgoing interleaved data bytes (r1, ..., r10); and

d. modulating means (MOD) provided to modulate said outgoing interleaved data stream (OID) on at least one data carrier to be transmitted over said transmission line (TL),

said interleaving means (INTERLEAVER) comprising:

c1. first memory means (MEM) including a plurality of first- in- first-out queues (Fifo0, Fifo1, Fifo2, Fifo3, Fifo4) adapted to represent respective rows of a first triangular shaped matrix (MAT) of memory cells;

c2. first writing means (WRITE) with an output coupled to an input of said first memory means (MEM), said first writing means (WRITE) being adapted to write each one of said incoming data bytes (w1, ..., w10) in a tail memory cell of one of said rows identified by a write address;

c3. first reading means (READ) with an input coupled to an output of said first memory means (MEM), said reading means (READ) being adapted to read each one of said outgoing interleaved data bytes (r1, ..., r10) from a head memory cell of one of said rows identified by a read address; and

c4. first address generating means (ADDRESS), a first output of which is coupled to an address input (AI1) of said first writing means (WRITE) and a second output of which is coupled to an address input (AI2) of said first reading means (READ), said first address generating means (ADDRESS) being adapted to generate said write address and said read address,

and said receiver (RX) comprising the cascade connection of:

e. de-modulating means (DMOD) provided to de-modulate incoming interleaved data bytes (w1', ..., w10') from said at least one carrier to thereby produce an incoming interleaved data stream (IID);

f. de-interleaving means (DE-INTERLEAVER) provided to re-sequence said incoming interleaved data bytes (w1', ..., w10') in said incoming interleaved data stream (IID) to thereby generate an outgoing data stream (OD) of outgoing data bytes (r1', ..., r10') grouped in codewords;

g. decoding means (DECODER) provided to detect and correct errors in said codewords by interpretation of redundant information therein to thereby produce a data stream of words; and

h. a data sink (DATA SINK) provided to receive said data stream from said decoding means (DECODER),

said de-interleaving means (DE-INTERLEAVER) comprising:

f1. second memory means (MEM') includ-

ing a plurality of first-in-first-out queues (Fifo0', Fifo1', Fifo2', Fifo3', Fifo4') adapted to represent respective rows of a second triangular shaped matrix (MAT') of memory cells;

f2. second writing means (WRITE') with an output coupled to an input of said second memory means (MEM'), said second writing means (WRITE') being adapted to write each one of said incoming interleaved data bytes (w1', ..., w10') in a tail memory cell of one of said rows identified by a write address;

f3. second reading means (READ') with an input coupled to an output of said second memory means (MEM'), said reading means (READ') being adapted to read each one of said outgoing data bytes (r1', ..., r10') from a head memory cell of one of said rows identified by a read address; and

f4. second address generating means (ADDRESS'), a first output of which is coupled to an address input (AI1') of said second writing means (WRITE') and a second output of which is coupled to an address input (AI2') of said second reading means (READ'), said second address generating means (ADDRESS') being adapted to generate said write address and said read address,

CHARACTERISED IN THAT said first address generating means (ADDRESS) is further adapted to generate for each row an amount of read addresses which is linearly related to an ordinate number (0, 1, 2, 3, 4) of said row in said first triangular shaped matrix (MAT), and further in that said second address generating means (ADDRESS') further is adapted to generate for each row of said second triangular shaped matrix (MAT') an amount of write addresses which is linearly related to an ordinate number (0, 1, 2, 3, 4) of said row in said second triangular shaped matrix (MAT').

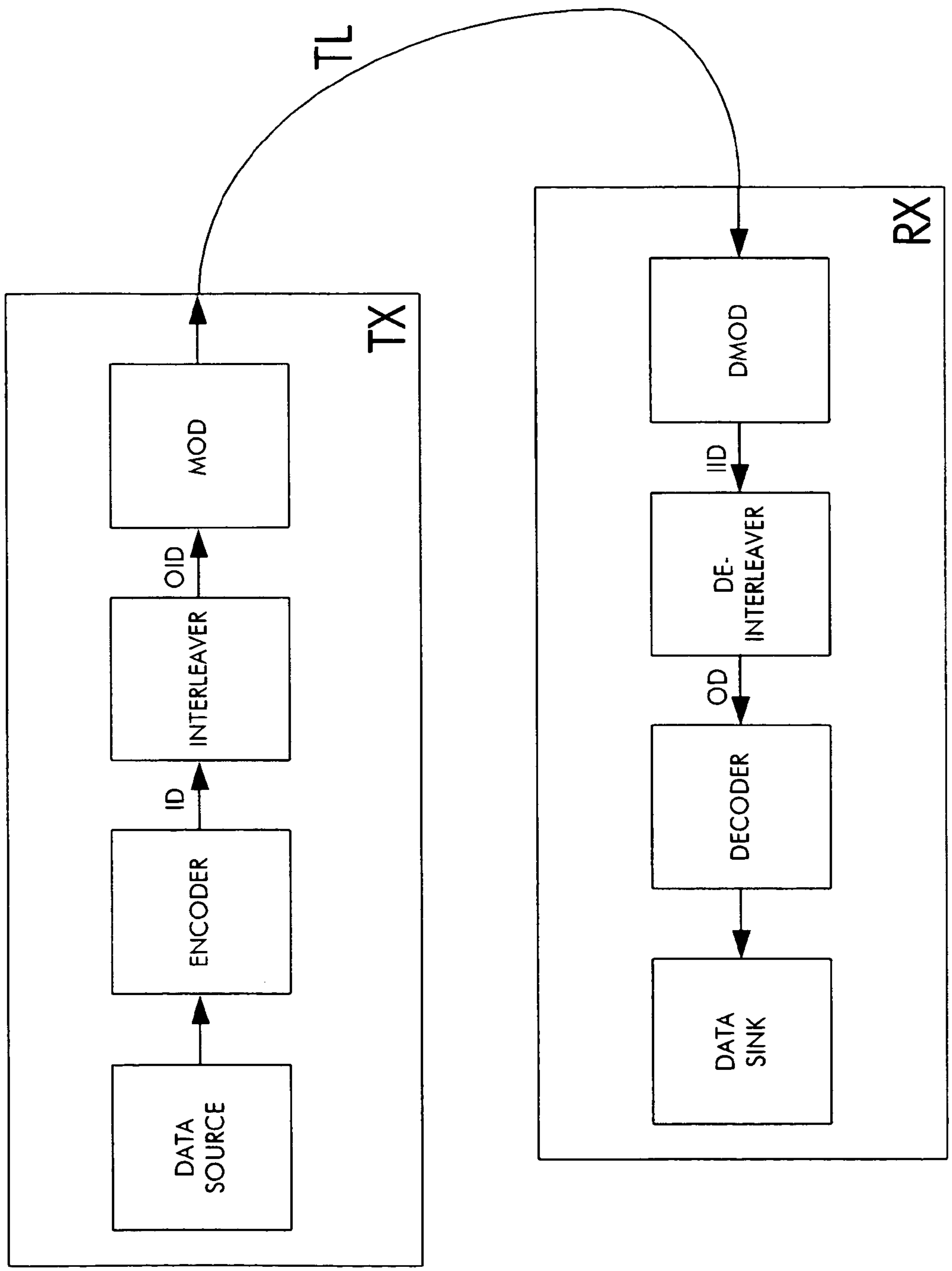
TL
TX
DATA SOURCE
ENCODER
ID
INTERLEAVER
OID
MOD
RX
DMOD
IID
DE-INTERLEAVER
OD
DECODER
DATA SINK

Fig. 1

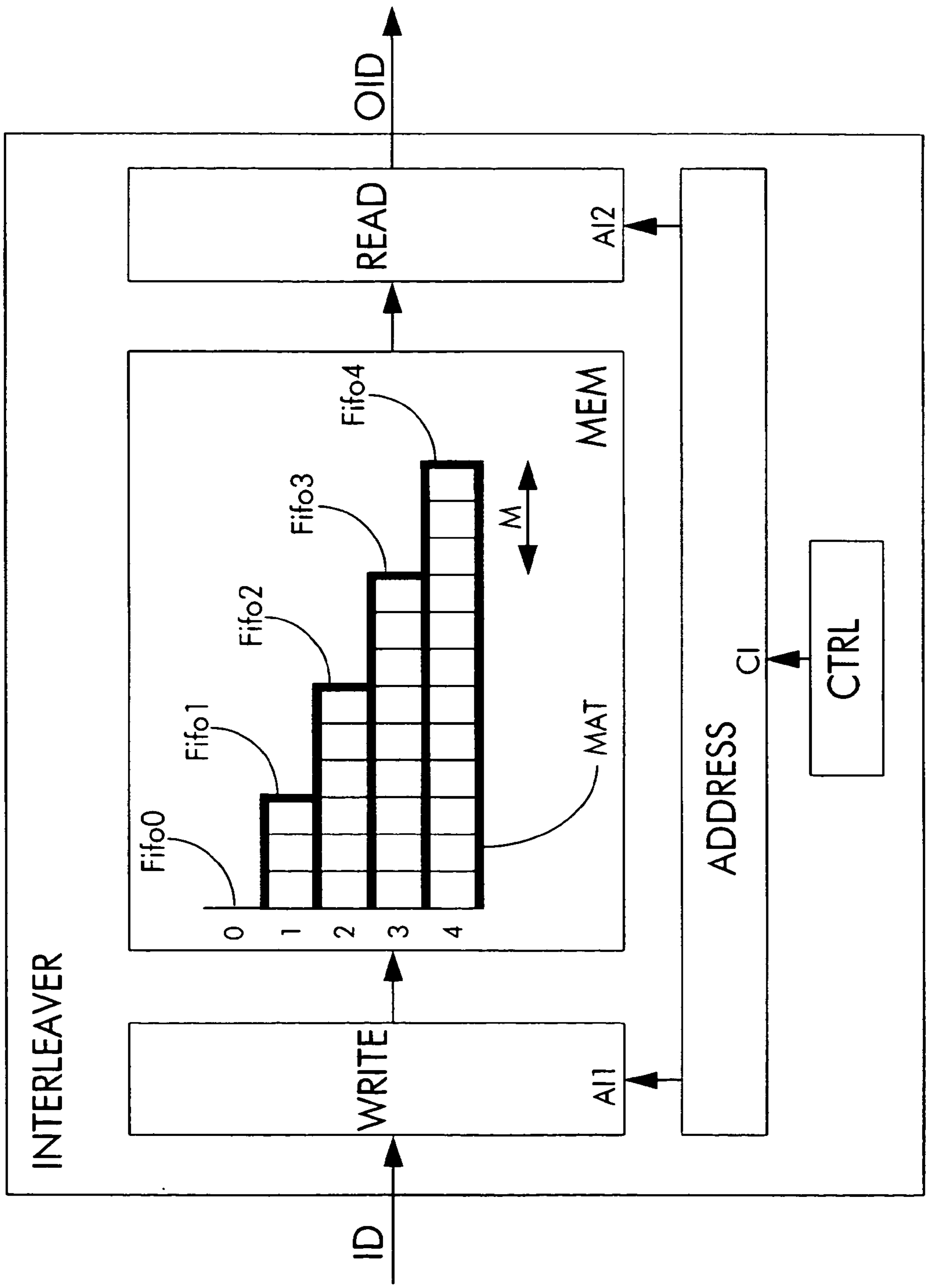
ID
INTERLEAVER
WRITE
AI1
MEM
0
1
2
3
4
Fifo0
Fifo1
Fifo2
Fifo3
Fifo4
MAT
M
READ
AI2
OID
ADDRESS
CI
CTRL

Fig. 2

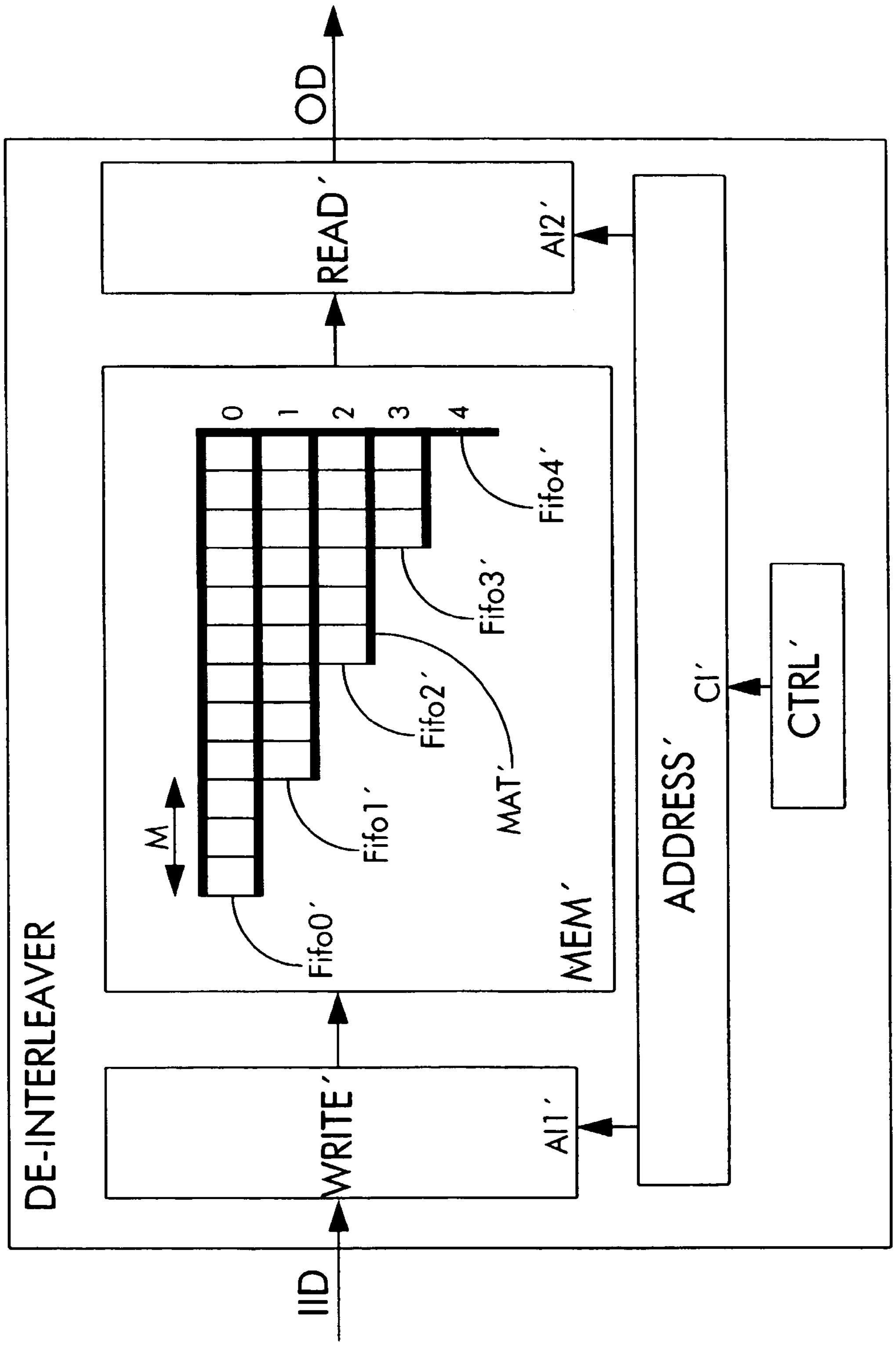
OD
DE-INTERLEAVER
READ´
AI2´
WRITE´
AI1´
MEM´
0
1
2
3
4
M
Fifo0´
Fifo1´
Fifo2´
Fifo3´
Fifo4´
MAT´
ADDRESS´
CI´
CTRL´
IID

Fig. 3

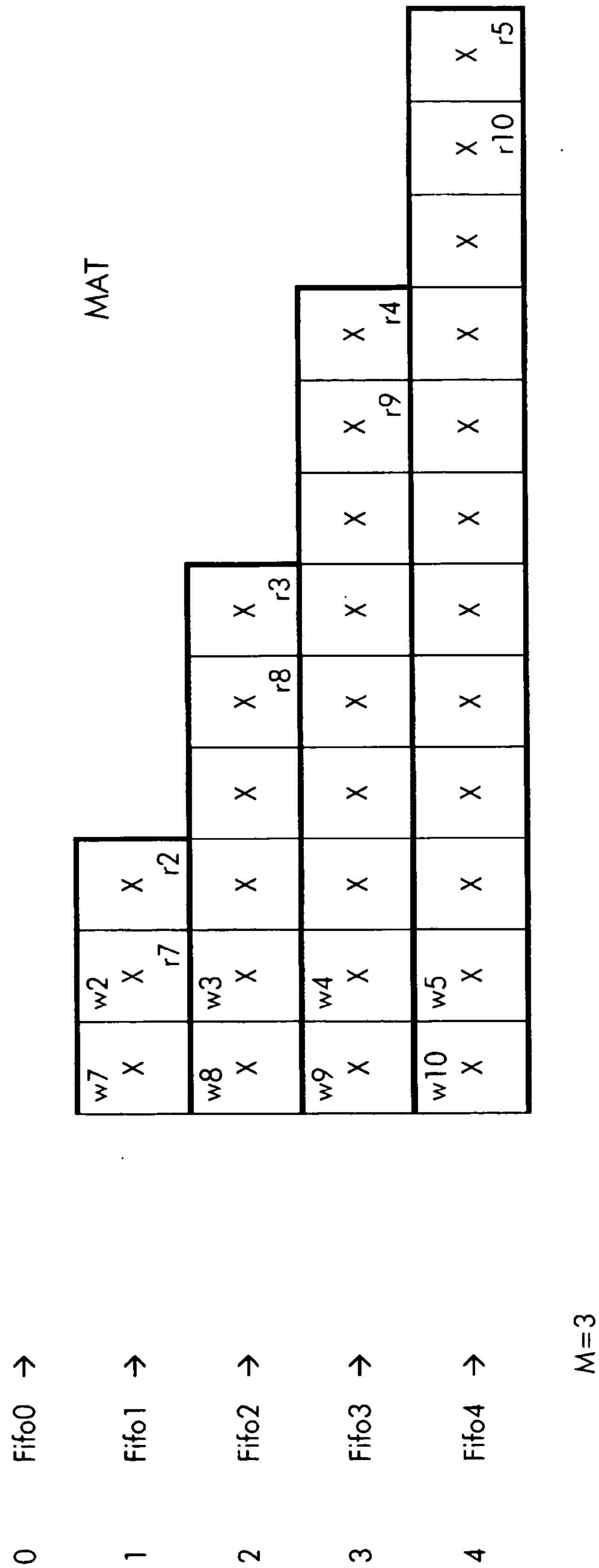
MAT
0 Fifo0
1 Fifo1
2 Fifo2
3 Fifo3
4 Fifo4
M=3
w7
w2
w8
w3
w9
w4
w10
w5
r7
r2
r8
r3
r9
r4
r10
r5

Fig. 4A

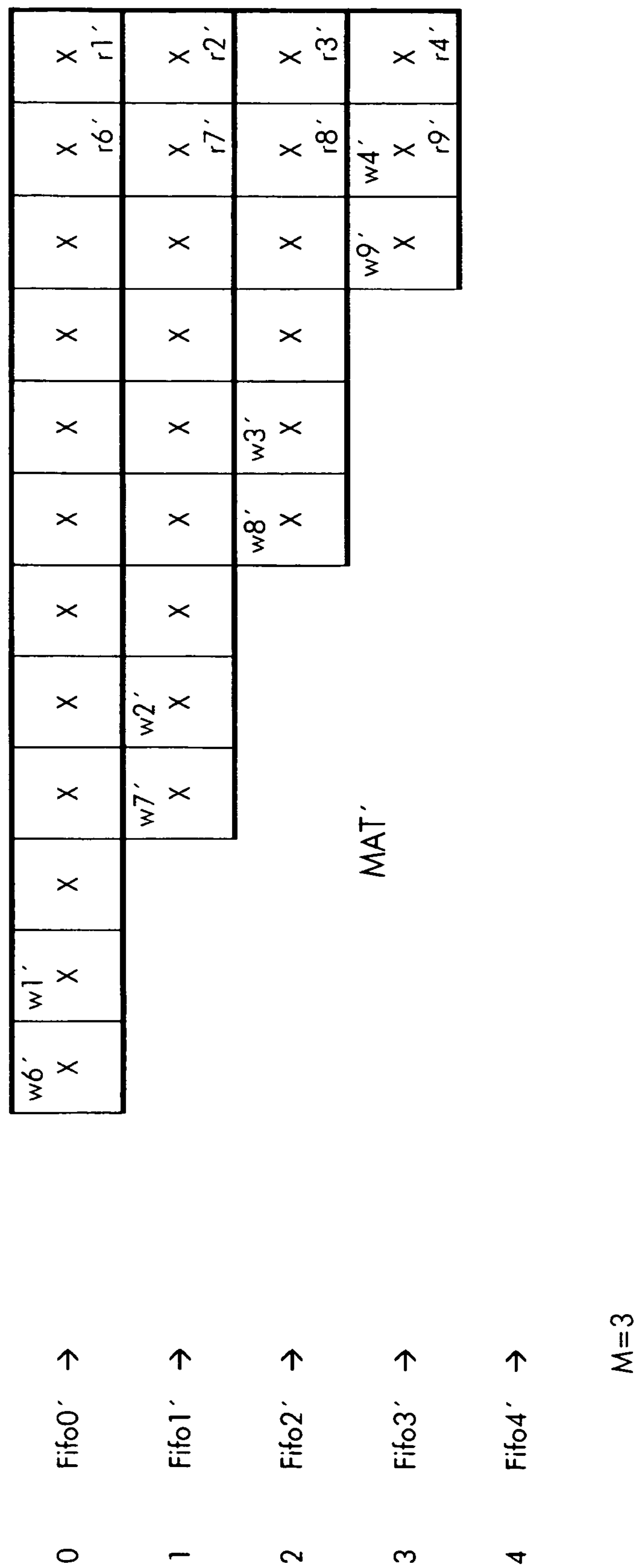
0 Fifo0'
1 Fifo1'
2 Fifo2'
3 Fifo3'
4 Fifo4'
M=3
MAT'
w6'
w1'
w7'
w2'
w8'
w3'
w9'
w4'
r1'
r2'
r3'
r4'
r6'
r7'
r8'
r9'

Fig. 4B

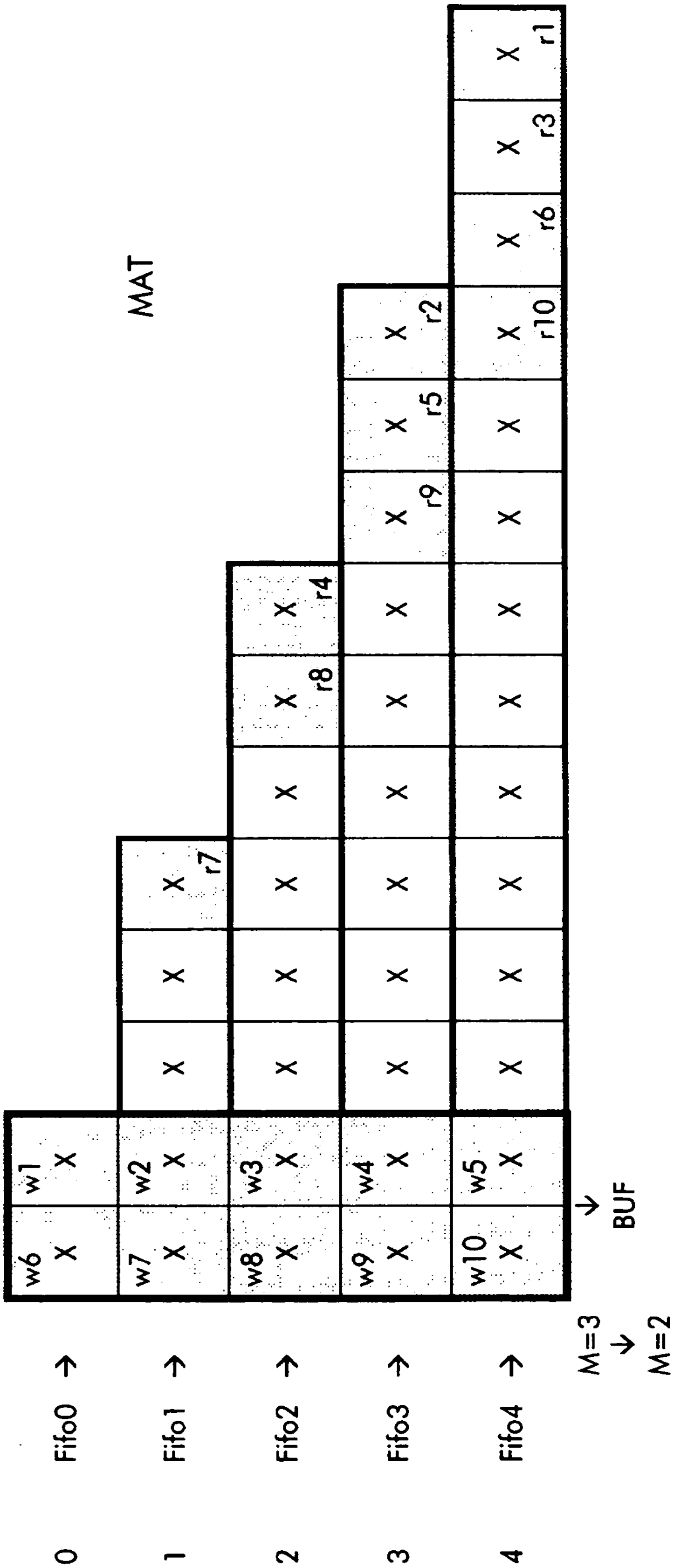
MAT
0 Fifo0
1 Fifo1
2 Fifo2
3 Fifo3
4 Fifo4
w1 w2 w3 w4 w5
w6 w7 w8 w9 w10
r1 r2 r3 r4 r5 r6 r7 r8 r9 r10
BUF
M=3 → M=2

Fig. 5A

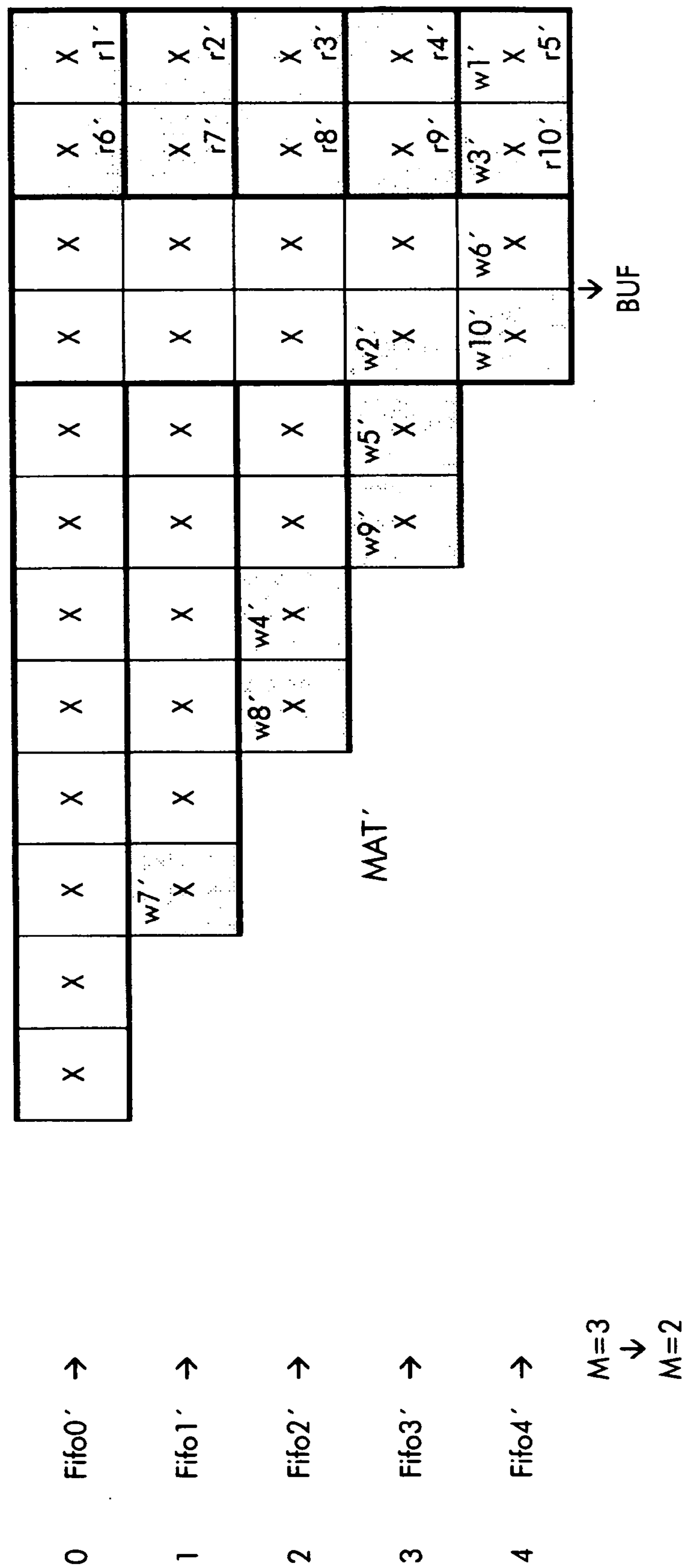
0 Fifo0'
1 Fifo1'
2 Fifo2'
3 Fifo3'
4 Fifo4'
M=3 → M=2
MAT'
BUF
r1' r2' r3' r4' r5'
r6' r7' r8' r9' r10'
w1' w2' w3' w4' w5' w6' w7' w8' w9' w10'

Fig. 5B

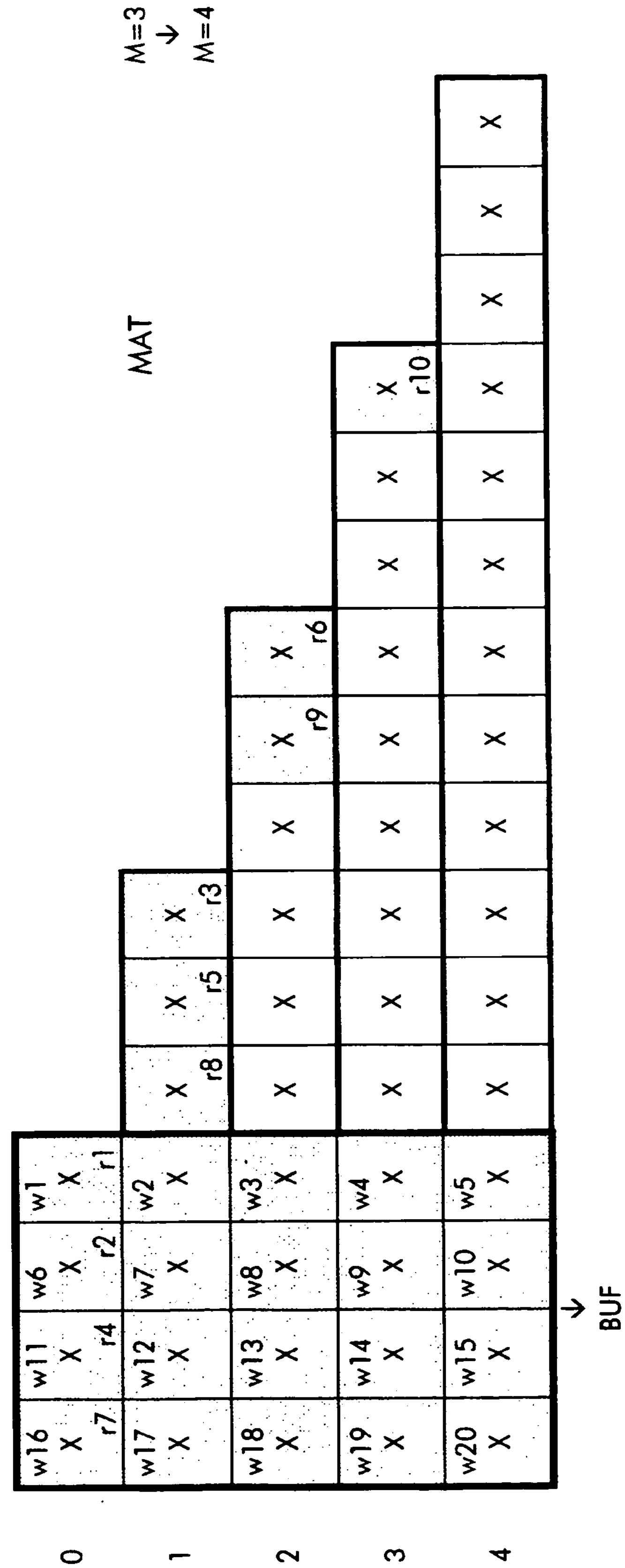
M=3 → M=4
MAT
BUF
0
1
2
3
4
w1 w6 w11 w16
w2 w7 w12 w17
w3 w8 w13 w18
w4 w9 w14 w19
w5 w10 w15 w20
r1 r2 r4 r7
r8 r5 r3
r9 r6
r10

Fig. 6A

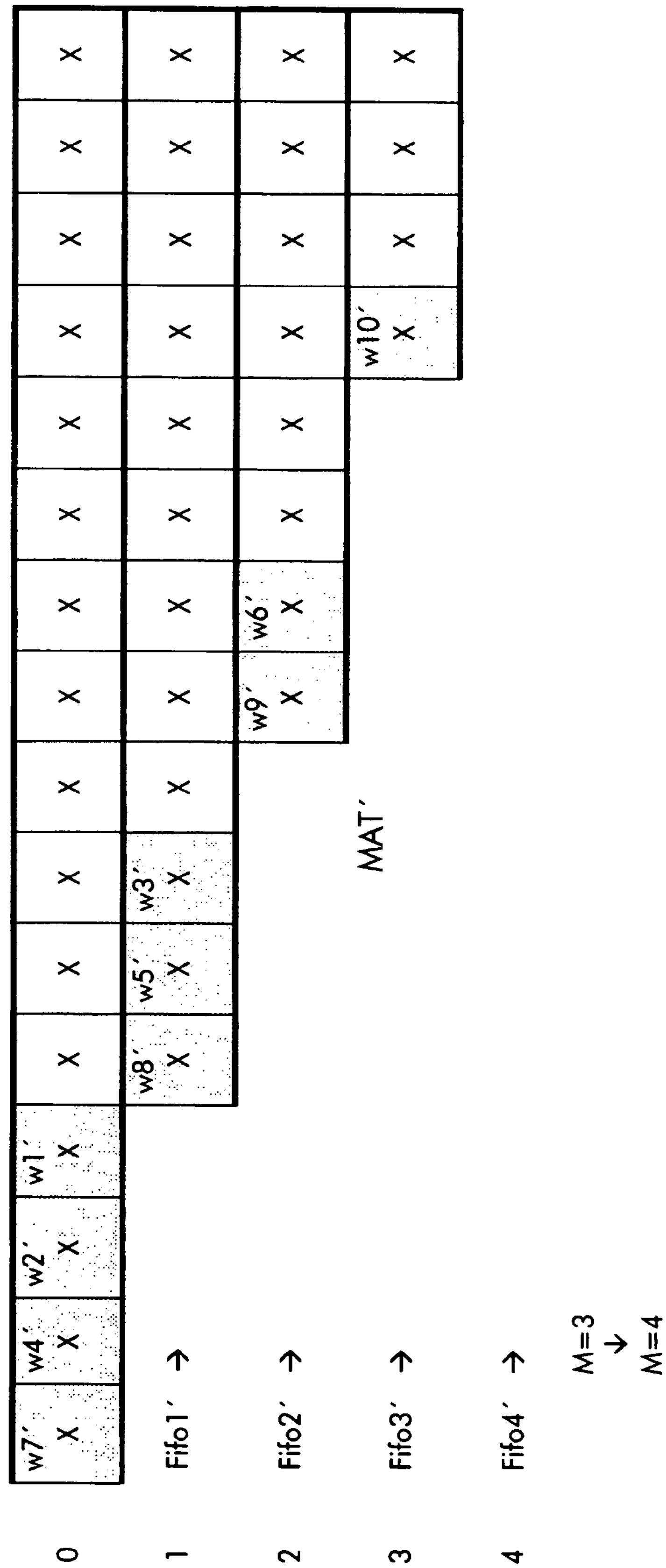
0
1
2
3
4
Fifo1'
Fifo2'
Fifo3'
Fifo4'
w7'
w4'
w2'
w1'
w8'
w5'
w3'
w9'
w6'
w10'
MAT'
M=3
M=4

Fig. 6B

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 97 40 0231

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
Y	FR 2 592 258 A (THOMSON)	1,11,12, 15,18	H03M13/00 H03M13/22
A	* page 3, line 32 - page 10, line 13; figures * ---	2-10,13, 14,16,17	
Y	EP 0 048 151 A (TOSHIBA) * page 5, line 1 - page 13, line 28; figures * ---	1,11,12, 15,18	
A	EP 0 681 373 A (GENERAL INSTRUMENT CORP.) * page 4, column 6, line 9 - page 7, column 11, line 20; figures * -----	1,11,12, 15,18	
			TECHNICAL FIELDS SEARCHED (Int.Cl.6)
			H03M G11B

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	4 July 1997	Geoghegan, C

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

Dispositif d'émission/réception de données numériques capable de traiter des débits différents, en particulier dans un environnement VDSL.

L'invention concerne d'une façon générale l'émission et la réception de données numériques pouvant présenter des débits différents, et plus particulièrement le dimensionnement des moyens de mémoire utilisés dans les traitements d'entrelacement et de désentrelacement effectués au sein de ces dispositifs d'émission/réception capables de traiter ces débits différents.

L'invention s'applique avantageusement et non limitativement à un environnement de lignes d'abonnés numériques à très haut débit encore dénommé par l'homme du métier, "environnement ou système de communication VDSL" (Very High Rate Digital Subscriber Line en langue anglaise), qui est un système de communication numérique entre un opérateur et des utilisateurs par l'intermédiaire de lignes de transmission à très haut débit.

L'invention s'applique ainsi plus particulièrement aux dispositifs d'émission/réception, encore couramment dénommé "Modem", disposés du côté opérateur et du côté utilisateur aux extrémités de la ligne de transmission.

L'homme du métier sait qu'un système de communication VDSL est capable de délivrer des services dits "symétriques" et des services dits "asymétriques". Un service est dit "symétrique" lorsque les débits d'information échangés entre l'opérateur et l'utilisateur sont identiques dans un sens de transmission et dans l'autre (c'est-à-dire de l'opérateur vers l'utilisateur et de l'utilisateur vers l'opérateur).

Un service est dit "asymétrique" lorsque le débit des informations dans un sens de transmission est différent du débit des

informations dans l'autre sens de transmission.

Les traitements d'entrelacement et de désentrelacement des données émises et reçues par un modem nécessitent l'utilisation de mémoires qui doivent être dimensionnées, pour un modem destiné à fonctionner selon un débit prédéterminé, en fonction dudit débit.

L'invention vise à proposer une architecture de dispositif d'émission/réception (modem) qui puisse s'adapter côté opérateur ou côté utilisateur (en d'autres termes, un tel modem est alors parfaitement interchangeable entre l'émission et la réception), et qui soit capable, notamment au niveau de la mémoire des moyens d'entrelacement et de désentrelacement, de s'adapter à un certain nombre de débits différents pris parmi un groupe prédéterminé de débits, tout en offrant une réduction de la taille-mémoire.

L'invention propose ainsi notamment d'utiliser des moyens de mémoire dont la taille est optimisée à partir d'un débit global (émission+réception), qui puissent être partagés entre les moyens d'entrelacement et les moyens de désentrelacement, et qui soient reconfigurables au niveau des allocations mémoire, en fonction du débit effectivement traité par le dispositif d'émission/réception (modem).

L'invention propose donc un dispositif d'émission/réception de données numériques, capable de traiter des débits différents pris parmi un groupe de débits prédéterminés (par exemple tous les services symétriques ou asymétriques proposés par le système de communication VDSL).

Le dispositif selon l'invention comprend un étage de codage/décodage (généralement dénommés par l'homme du métier "étage de codage/décodage de canal") comportant des moyen d'entrelacement et des moyens de désentrelacement. Ces moyens d'entrelacement et de désentrelacement incluent une mémoire dont la taille minimale est fixée en fonction du débit maximal dudit groupe (par exemple le plus grand débit asymétrique dans le cas d'un système VDSL). Par ailleurs, cette mémoire possède un premier espace-mémoire alloué aux moyens d'entrelacement et un deuxième espace-mémoire alloué aux moyens de désentrelacement. La taille de chacun des deux espaces-mémoire est paramétrable en fonction du débit effectivement traité par le dispositif.

Au sens de la présente invention, le terme "débit" associé à un dimensionnement de mémoire ou d'espace-mémoire s'entend comme étant un débit global, c'est-à-dire la somme des débits en réception et en émission.

Il est ainsi possible de réduire considérablement la taille des moyens de mémoire requis pour les moyens d'entrelacement et de désentrelacement lorsque ces moyens sont réalisés au sein d'un modem capable d'être disposé au choix côté opérateur ou côté utilisateur, et capable de pouvoir traiter au choix plusieurs débits différents symétriques ou asymétriques.

Généralement, le flot de transmission de données est protégé vis-à-vis des bruits du canal de transmission par un algorithme de codage du type Reed-Solomon, bien connu de l'homme du métier. Afin d'augmenter l'efficacité du codage de Reed-Solomon, celui-ci est couplé aux moyens d'entrelacement afin de répartir dans le temps les erreurs introduites par le canal de transmission, qui se produisent souvent en rafale affectant plusieurs octets successifs, pouvant ainsi réduire la capacité de correction du codage Reed-Solomon seul (en général huit octets par paquet). Les moyens d'entrelacement procèdent alors à un entrelacement temporel des octets en modifiant leur ordre de transmission, ce qui permet d'obtenir ladite répartition temporelle des erreurs.

Plus précisément, selon un mode de réalisation de l'invention, l'étage de codage/décodage de canal comporte des moyens de codage et de décodage de Reed-Solomon de longueur N (N étant par exemple égal à 240 octets). Les moyens d'entrelacement sont alors aptes à mettre en oeuvre un entrelacement triangulaire convolutif à I branches de i-1 blocs de M octets. Les moyens de désentrelacement sont quant à eux aptes à mettre en oeuvre un désentrelacement convolutif triangulaire à I' branches de i'-1 blocs de M' octets. I et I' sont des sous-multiples de N et i et i' désignent les indices relatifs courants des branches. Par ailleurs, la taille en octets du premier espace-mémoire est égale à Ix(I-1)xM/2, tandis que la taille en octets du deuxième espace-mémoire est égale à I'x(I'-1)xM'/2. Et, la taille de ces deux espaces-mémoire est paramétrable par I, I', M et M'.

L'utilisation d'un entrelacement triangulaire convolutif (et par

conséquent d'un désentrelacement triangulaire convolutif) au lieu d'un autre type d'entrelacement classique, est particulièrement intéressant car il permet de diminuer la latence engendrée par la mémoire. En effet, un entrelacement triangulaire convolutif nécessite un espace-mémoire moins important, ce qui permet une diminution de la latence. Et, cette latence est un critère primordial et décisif pour un système de communication VDSL.

Selon un mode de réalisation particulièrement simple, la mémoire est une mémoire vive, par exemple à double accès. Les moyens d'entrelacement et de désentrelacement comprennent respectivement des premier et deuxième moyens d'adressage. Chacun de ces premier et deuxième moyens d'adressage comprennent :

- un premier compteur définissant l'indice relatif i ou i' d'une branche,
- un deuxième compteur définissant le nombre d'octets dans un bloc, ce deuxième compteur étant incrémenté à chaque fois que le premier compteur a atteint sa valeur limite de comptage,
- un troisième compteur définissant l'indice courant d'un bloc dans la branche d'indice i ou i', ce troisième compteur étant incrémenté à chaque fois qu'un bloc contient M ou M' octets, et
- des moyens de calcul intermédiaires, calculant l'adresse de chaque branche dans ladite mémoire à partir du contenu du premier compteur, c'est-à-dire à partir de l'indice relatif i ou i'.

Par ailleurs, les premiers moyens d'adressage (relatifs aux moyens d'entrelacement) comportent en outre des premiers moyens de détermination d'adresse, aptes à déterminer les adresses successives de lecture et d'écriture dans la mémoire des données successivement délivrées au moyen d'entrelacement. Ces premiers moyens de détermination d'adresse déterminent lesdites adresses à partir des valeurs fournies par les moyens de calcul intermédiaires, les deuxième et troisième compteurs, et à partir du paramètre M.

Par ailleurs, les deuxièmes moyens d'adressage (c'est-à-dire ceux relatifs aux moyens de désentrelacement) comportent en outre des deuxièmes moyens de détermination d'adresse, aptes à déterminer les adresses successives de lecture et d'écriture dans ladite mémoire des

données successivement délivrées aux moyens de désentrelacement. Ces deuxièmes moyens de détermination d'adresse déterminent lesdites adresses à partir des valeurs fournies par les moyens de calcul intermédiaires, les deuxième et troisièmes compteurs, et à partir du paramètre M', et de la taille du premier espace-mémoire (ce qui permet ainsi de déterminer la première adresse non occupée dans la mémoire).

D'autres avantages et caractéristiques de l'invention apparaîtront à l'examen de la description détaillée de modes de réalisation, nullement limitatifs, et des dessins annexés, sur lesquels :

- la figure 1 illustre très schématiquement un système de communication entre deux dispositifs d'émission/réception, selon l'invention;
- la figure 2 illustre plus en détail mais toujours schématiquement, l'architecture interne d'un dispositif d'émission/ réception, selon l'invention;
- la figure 3 illustre schématiquement mais plus en détail l'architecture interne d'un étage de codage/décodage du dispositif de la figure 2;
- les figures 4 et 5 illustrent schématiquement les principes de mise en oeuvre d'un entrelacement et d'un désentrelacement triangulaires convolutifs;
- la figure 6 illustre plus en détail, mais toujours schématiquement, l'architecture interne des moyens d'entrelacement et de désentrelacement d'un dispositif d'émission/réception, selon l'invention;
- la figure 7 illustre schématiquement un mode de réalisation des premiers moyens d'adressage associés aux moyens d'entrelacement; et
- la figure 8 illustre schématiquement un exemple de réalisation des deuxièmes moyens d'adressage associés aux moyens de désentrelacement.

On va maintenant décrire une application de l'invention à un système de communication VDSL, bien que l'invention n'y soit pas limitée.

Ainsi, sur la figure 1, les références TO et TU désignent deux dispositifs d'émission/réception selon l'invention, encore désignés plus simplement terminaux ou modem. L'un de ces terminaux, par exemple le

terminal TO, est situé côté opérateur, tandis que l'autre terminal TU est situé côté utilisateur. Ces deux modems sont reliés par une ligne de communication LH à très haut débit.

Ainsi, à titre indicatif, le système de communication VDSL permet à l'opérateur d'offrir des services symétriques, typiquement six services symétriques S1-S6, c'est-à-dire des services dont les débits d'informations dans un sens de transmission ou dans l'autre (de l'opérateur vers l'utilisateur ou de l'utilisateur vers l'opérateur) sont identiques. A titre d'exemple, le service S1 qui présente le plus faible débit a un débit de 32x64 kbits/seconde, tandis que le service symétrique le plus rapide S6 a un débit de 362x64 kbits/seconde.

Avec le système VDSL, l'opérateur peut également fournir des services dits "asymétriques" A1-A6, c'est-à-dire présentant des débits d'informations différents dans le sens utilisateur-opérateur (sens montant) et dans le sens opérateur-utilisateur (sens descendant).

Ainsi, à titre indicatif, le premier service asymétrique A1 offert possède un débit dans le sens montant de 32x64 kbits/seconde et un débit dans le sens descendant de 100x64 kbits/seconde.

Le service asymétrique possédant le plus grand débit global d'informations (débit montant + débit descendant) est le service A6 dont le débit dans le sens montant est égal à 32x64 kbits/seconde et dont le débit dans le sens descendant est égal à 832x64 kbits/seconde.

Le dispositif d'émission/réception selon l'invention, va ainsi pouvoir être disposé côté utilisateur ou côté opérateur et va être capable de traiter tous ces services moyennant, comme on va le voir plus en détail ci-après, un dimensionnement de la mémoire affectée aux moyens d'entrelacement/désentrelacement en fonction du débit maximum parmi les services proposés, en l'espèce le débit du plus grand service asymétrique (service A6), et moyennant un paramétrage de l'espace-mémoire de cette mémoire en fonction du service effectivement traité par le dispositif.

On va maintenant décrire plus en détail l'architecture interne de l'un des terminaux de la figure 1 (en l'espèce le terminal opérateur TO), étant bien entendu que tout ce qui va être décrit ci-après est valable pour le terminal TU.

Le terminal TO comporte (figure 2) une chaîne d'émission et une chaîne de réception, toutes les deux reliées à la ligne de transmission LH.

L'un des constituants du terminal TO est un étage ETC de codage/décodage de canal comportant, au niveau de la chaîne d'émission un bloc de codage de canal CC et au niveau de la chaîne de réception un bloc de décodage de canal DCC.

Le bloc de codage de canal CC comporte notamment des moyens de codage de Reed-Solomon, dont la structure et la fonction sont bien connues de l'homme du métier. Ces moyens de codage de Reed-Solomon sont associés à des moyens d'entrelacement.

Plus précisément, le codage de Reed-Solomon permet avec l'entrelacement qui le suit, la correction des erreurs en rafale introduites par le canal de transmission. Le codage de Reed-Solomon s'applique individuellement à chacun des paquets de données délivrés en entrée du bloc de codage CC. Le codage de Reed-Solomon ajoute un certain nombre d'octets de parité aux octets des paquets reçus et permet ainsi de corriger un certain nombre d'octets erronés. On suppose ici, à titre d'exemple, que le codage de Reed-Solomon réalisé est un codage RS (240, 224) avec un pouvoir correcteur de 8. Ceci signifie que les moyens de codage de Reed-Solomon s'appliquent sur des paquets de 224 octets et y rajoutent 16 octets de parité, de façon à former un mot codé de Reed-Solomon dont la longueur est de 240 octets. Et, il est possible ainsi de corriger jusqu'à 8 octets erronés.

Puis, afin de répartir dans le temps les erreurs introduites par le canal qui se produisent souvent en rafale affectant plusieurs octets successifs, pouvant ainsi excéder la capacité de correction du codage de Reed-Solomon seule, on procède, afin d'augmenter l'efficacité de ce codage de Reed-Solomon, à un entrelacement temporel des octets en modifiant leur ordre de transmission.

Les informations délivrées à la sortie de l'étage de codage de canal ETC, sont délivrées à un bloc de modulation BM de structure classique et connue en soi, qui peut par exemple effectuer une modulation en quadrature. Puis, après différents traitements classiques effectués dans un bloc d'émission EM comportant notamment une interface avec la ligne de transmission LH, le signal modulé est transmis sur cette ligne de

transmission LH.

D'une façon analogue, la chaîne de réception du terminal TO comporte en tête un bloc de réception ER comportant notamment une interface de réception avec la ligne de transmission LH et effectuant des traitements classiques. Le signal modulé délivré à la sortie du bloc de réception ER est démodulé dans un bloc de démodulation BDM, puis le signal démodulé est délivré au bloc de décodage de canal DCC. Celui-ci comporte ainsi notamment des moyens de désentrelacement et des moyens de décodage de Reed-Solomon.

On se réfère maintenant plus particulièrement aux figures 3 et suivantes, pour décrire plus en détail l'architecture interne et le fonctionnement des moyens d'entrelacement et de désentrelacement.

Comme illustré sur la figure 3 et déjà expliqué plus haut, les moyens d'entrelacement MET font suite à des moyens de codage de Reed-Solomon CRS, tandis que les moyens de désentrelacement MDET précèdent des moyens de décodage DCRS de Reed-Solomon.

Comme illustré schématiquement sur les figures 4 et 5, l'entrelacement et le désentrelacement réalisés sont un entrelacement et un désentrelacement triangulaires convolutifs à I branches de i-1 blocs de M octets en ce qui concerne l'entrelacement, et à I' branches de i'-1 blocs de M' octets, en ce qui concerne le désentrelacement.

Comme on le verra plus en détail ci-après, les paramètres I et M d'une part, et I' et M' d'autre part, sont modifiables par exemple par logiciel, et sont délivrés par des moyens de commande MCD (figure 3) qui peuvent être des moyens logiciels. Ces paramètres définissent les tailles des espaces-mémoire qui vont être respectivement allouées aux moyens d'entrelacement et aux moyens de désentrelacement en fonction du débit des informations émises par le terminal TO (paramètres I et M) et du débit des informations reçues par le terminal TO (paramètres I' et M').

Sur la figure 4, I a été choisi à titre d'exemple égal à 7. Les moyens d'entrelacement comportent donc I branches parallèles BRi (numérotées par exemple de 0 à I-1) qui sont réalisées avec un incrément de retard de M par branche (M représente le nombre maximal d'octets d'un bloc BKj d'indice j). Chaque branche peut être considérée comme une ligne à retard, la longueur de la branche d'indice i avec i variant de 0 à I-1,

étant égale à ixM octets.

Ainsi, le premier bloc (ayant par exemple l'indice 0) de M octets n'est pas entrelacé et est délivré tel quel en sortie des moyens d'entrelacement. Le bloc suivant (ayant l'indice 1) de M octets est délivré à l'entrée de la branche BR1 et ainsi de suite jusqu'à ce que le septième bloc de M octets (ayant l'indice 6) soit délivré à la branche BR6. Puis, le cycle recommence avec les blocs d'octets d'indices 7 à 13, les blocs d'octets précédents étant soit délivrés en sortie des moyens d'entrelacement, soit progressant d'un bloc BKj dans la branche considérée.

Les moyens de désentrelacement associés à ces moyens d'entrelacement MET, et qui sont par conséquent incorporés dans le terminal utilisateur TU, ont une structure analogue à celle qui vient d'être décrite pour les moyens d'entrelacement, mais les indices de branches sont inversés de telle sorte que le plus grand retard d'entrelacement corresponde au plus petit retard de désentrelacement.

En ce qui concerne les moyens de désentrelacement MDET incorporés dans le terminal de l'opérateur TO, ils comprennent I' branches, la branche d'indice i' ayant une longueur égale à i'xM' octets.

Sur la figure 5, on a représenté à des fins de simplification I'=I, mais bien entendu, si le service est un service asymétrique, I et I' sont généralement différents, de même que M et M'.

Matériellement, comme illustré schématiquement sur la figure 6, les moyens d'entrelacement et les moyens de désentrelacement comprennent des moyens de mémoire communs MM, formés par exemple d'une mémoire vive à double accès. L'espace-mémoire de cette mémoire MM se décompose alors en un premier espace-mémoire ESM1 alloué aux moyens d'entrelacement MET et en un deuxième espace-mémoire ESM2 alloué aux moyens de désentrelacement MDET.

Les moyens d'entrelacement comportent par ailleurs des premiers moyens d'adressage MAD1 recevant les paramètres I et M, tandis que les moyens de désentrelacement comportent des deuxièmes moyens d'adressage MAD2 recevant les paramètres I' et M'. La structure de ces moyens d'adressage sera décrite plus en détail ci-après en référence aux figures 7 et 8.

La taille minimale de la mémoire MM est fixée en fonction du débit maximal pouvant être traité par le dispositif d'émission/réception. Par débit maximal, on entend bien entendu la somme du débit montant et du débit descendant.

En l'espèce, le débit maximal est fourni ici par le plus grand service asymétrique A6.

On va maintenant donner, à titre d'exemple non limitatif, un exemple de dimensionnement de la mémoire MM et du choix des paramètres I, M, I' et M' pour un service asymétrique A6 et un codage de Reed-Solomon RS (240, 224) avec un pouvoir de correction de 8 octets/mot et en faisant l'hypothèse que les lignes de transmission sont perturbées par un bruit impulsif de 0,250 ms.

Dans le sens descendant, le débit maximum est égal à 832x64 kbits/seconde.

Le nombre de bits bruités est par conséquent égal au produit de ce débit par la durée du bruit impulsif, ce qui fournit un nombre de bits bruités égal à 13312 (1664 octets). Compte tenu du pouvoir correcteur du codage de Reed-Solomon (ici 8), le nombre nrs de mots de Reed-Solomon nécessaires pour corriger 1664 octets bruités est égal à 1664/8, soit 208.

La taille de l'espace-mémoire pour stocker un tel débit maximum est alors égale à N.nrs/2 où N est la taille du codage de Reed-Solomon (ici 240).

Il en résulte donc une taille de l'espace-mémoire correspondant égale à 24960 octets.

Le débit dans le sens montant est égal à 32x64 kbits/seconde. Un calcul analogue montre que le nombre de bits bruités est égal à 512 et que nrs=8. Il en résulte alors une taille d'espace-mémoire à prévoir pour le sens montant égale à 1920 octets. La taille minimale de la mémoire MM est donc de 26880 octets.

Compte tenu de ces tailles, il est possible de déterminer les paramètres I, I', M et M'. Plus précisément, la taille du premier espace-mémoire nécessaire pour mettre en oeuvre un entrelacement convolutif triangulaire à I branches de i-1 blocs de M octets est égale à Ix(I-1)xM/2.

De même, la taille du deuxième espace-mémoire ESM2 destiné à supporter le débit montant est égale à I'x(I'-1)xM'/2.

Par ailleurs, I et I' doivent être des sous-multiples de la taille N du codage de Reed-Solomon.

Puisque Ix(I-1)xM/2 doit être égale à 24960, il est possible de choisir I=40 et M=32. De même, puisque I'x(I'-1)xM'/2 doit être au moins égale à 1920, il est possible de choisir (moyennant une légère augmentation de cette taille pour atteindre 1932 afin de faciliter l'implémentation) I'=24 et M'=7.

La taille définitive de la mémoire MM est donc égale à 26892 octets.

Le calcul de I, M, I' et M', qui vient d'être fait pour le service asymétrique A6, peut être fait d'une façon analogue pour les autres services du système VDSL. On peut ainsi mémoriser dans l'étage de codage/décodage une table de valeurs pour les paramètres I, M, I' et M'. Lors de l'installation du modem en bout de ligne et en fonction du service effectivement fourni par l'opérateur, les moyens de contrôle MCD vont extraire de cette table mémorisée les valeurs correspondantes de I, M, I' et M', et les délivrer aux moyens d'adressage MAD1 et MAD2 dont la structure va maintenant être décrite plus en détail en se référant aux figures 7 et 8.

Sur la figure 7, on voit que les premiers moyens d'adressage comprennent un premier compteur CT1 délivrant, au rythme d'un signal d'horloge, l'indice relatif i d'une branche BRi. Cet indice i est délivré à des moyens de calcul intermédiaires MCI qui déterminent l'adresse adbs de la branche BRi dans le premier espace-mémoire. Plus précisément, cette adresse adbs est égale à ix(i-1)/2. La structure de ces moyens MCI peut être aisément formée de multiplieur, diviseur et soustracteur.

Le premier compteur CT1 a une plage de comptage égale à I et compte ainsi par exemple de 0 à I-1.

Les moyens MD1 comportent par ailleurs un deuxième compteur CT2 qui délivre une valeur courante m égale au nombre courant d'octets dans chaque bloque BKj d'une branche BRi. La plage de comptage de ce compteur CT2 est égale à M. En d'autres termes, m peut varier par exemple de 0 à M-1.

Le deuxième compteur CT2 est incrémenté d'une unité à chaque fois que i=I-1.

Les moyens MDA1 comportent également un troisième compteur CT3, qui délivre l'indice j du bloc BKj de la branche d'indice i. La plage de comptage de ce compteur CT3 est égale à i. En d'autres termes, j varie par exemple de 0 à i-1. Ce troisième compteur CT3 est incrémenté à chaque fois qu'un bloc contient M octets, c'est-à-dire en l'espèce à chaque fois par exemple que le compteur CT2 atteint la valeur M.

Les moyens MDA1 comportent également des premiers moyens de détermination d'adresse MD1, qui déterminent l'adresse de lecture ar dans la mémoire et l'adresse d'écriture aw dans la mémoire.

Plus précisément, l'adresse de lecture ar est égale à (adbs + j)xM + m.

L'adresse d'écriture aw est alors tout simplement égale à l'adresse de lecture, mais retardée d'un cycle du signal d'horloge.

Là encore, les moyens MD1 peuvent être aisément réalisables à partir d'additionneurs et de multiplieurs.

Par ailleurs, à titre d'exemple non limitatif, il est possible d'utiliser, pour stocker la valeur de l'indice j délivrée par le troisième compteur CT3, qui est incrémenté tous les M cycles d'horloge, une petite mémoire auxiliaire double accès dont la taille serait égale à (I-1)xM bits. Tous les M cycles d'horloge, la valeur du j correspond à la ième branche dans la mémoire auxiliaire, puis le compteur CT3 est incrémenté et la nouvelle valeur est réécrite à la même adresse.

La structure des deuxièmes moyens d'adresse MDA2 qui vont délivrer les adresses de lecture ar' et d'écriture aw' dans le deuxième espace-mémoire de la mémoire MM, ont une structure sensiblement analogue à celle qui vient d'être décrite pour les premiers moyens d'adresse MDA1. On va décrire ici que la différence entre les moyens MDA1 et les moyens MDA2.

Le premier compteur CT10 délivre l'indice relatif i' d'une branche. i' varie cette fois-ci de I'-1 à 0. Les moyens de calcul intermédiaires MCI délivrent l'adresse de chaque branche adbs' en utilisant une formule analogue à celle utilisée pour le calcul de l'adresse, mais en remplaçant i par i'.

Le deuxième compteur CT20 définit le nombre m' d'octets dans un bloc et est incrémenté à chaque fois que le compteur CT10 atteint sa

valeur limite de comptage, en l'espèce lorsque i' atteint la valeur 0. Le deuxième compteur CT20 varie ici de 0 à M'-1.

Le troisième compteur CT30 définit l'indice courant j' d'un bloc dans la branche d'indice i'. Il varie de 0 à i'-1 et est incrémenté à chaque fois qu'un bloc contient M' octets, c'est-à-dire lorsque le deuxième compteur CT20 a atteint la valeur M'.

Les deuxièmes moyens d'adressage MDA2 comportent des deuxièmes moyens de détermination d'adresse MD2 qui déterminent les adresses d'écriture aw' et ar'. Cependant, cette fois-ci, les moyens MD2 doivent tenir compte de la taille du premier espace-mémoire ESM1, cette taille OF est définie par la formule (1) ci-dessous :

$$OF = I x (I-1) x M/2 \qquad (1)$$

et est par exemple stockée dans un registre. En effet, pour l'entrelacement dans le sens montant, les adresses de la mémoire MM variaient de 0 à OF-1.

La première adresse non occupée dans la mémoire MM vaut donc OF.

Les moyens MD2 calculent alors l'adresse de lecture ar' selon la formule (2) ci-dessous :

$$ar' = OF + M' x (adbs' + j') + m' \qquad (2)$$

L'adresse d'écriture aw' est égale à l'adresse de lecture et est disponible au coup d'horloge suivant.

Bien entendu, tout ce qui vient d'être décrit ici pour le terminal TO s'applique au terminal TU avec des moyens de désentrelacement à I branches et des moyens d'entrelacement à I' branches. Il convient alors de remplacer, en ce qui concerne le terminal utilisateur TU, I par I' et vice versa, et M par M' et vice versa, dans tout ce qui précède.

En outre, il serait également possible d'utiliser une mémoire simple accès à la place d'une mémoire double accès, en adoptant un signal d'horloge de fréquence double.

REVENDICATIONS

1. Dispositif d'émission/réception de données numériques, capable de traiter des débits différents pris parmi un groupe de débits prédéterminés, comprenant un étage de codage/décodage de canal comportant des moyens d'entrelacement (MET) et des moyens de désentrelacement (MDET) incluant une mémoire (MM) dont la taille minimale est fixée en fonction du débit maximal dudit groupe, et possédant un premier espace-mémoire (ESM1) alloué aux moyens d'entrelacement et un deuxième espace-mémoire (ESM2) alloué aux moyens de désentrelacement, la taille de chacun de ces deux espaces-mémoire étant paramétrable en fonction du débit effectivement traité par le dispositif.

2. Dispositif selon la revendication 1, caractérisé par le fait que l'étage de codage/décodage de canal comportent des moyens de codage/ décodage de Reed-Solomon (CRS, DCRS) de longueur N, par le fait que les moyens d'entrelacement (MET) sont aptes à mettre en oeuvre un entrelacement convolutif à I branches de i-1 blocs de M octets, et les moyens de désentrelacement sont aptes à mettre en oeuvre un désentrelacement convolutif à I' branches de i'-1 blocs de M' octets, I et I' étant des sous-multiples de N et i et i' les indices relatifs courants des branches, par le fait que la taille en octets du premier espace-mémoire est égal à Ix(I-1)xM/2 et la taille en octets du deuxième espace-mémoire est égal à I'x(I'-1)xM'/2, et par le fait que les tailles de ces deux espaces-mémoire sont paramétrables par I, I', M et M'.

3. Dispositif selon la revendication 2, caractérisé par le fait que la mémoire (MM) est une mémoire vive en particulier à double accès, par le fait que les moyens d'entrelacement et de désentrelacement comprennent respectivement des premiers (MDA1) et des deuxièmes (MDA2) moyens d'adressage comportant chacun

un premier compteur (CT1, CT10) définissant l'indice relatif i ou i' d'une branche,

un deuxième compteur (CT2, CT20) définissant le nombre d'octets dans un bloc et incrémenté à chaque fois que le premier compteur atteint sa valeur limite de comptage,

un troisième compteur (CT3, CT30) définissant l'indice courant d'un bloc dans la branche d'indice i ou i', et incrémenté à chaque fois qu'un bloc contient M ou M' octets,

des moyens de calcul intermédiaires (MCI) calculant l'adresse (adbs, adbs') de chaque branche dans ladite mémoire à partir du contenu du premier compteur,

par le fait que les premiers moyens d'adressage (MDA1) comportent en outre des premiers moyens de détermination d'adresse (MD1) aptes à déterminer les adresses successives de lecture et d'écriture dans ladite mémoire, des données successivement délivrées aux moyens d'entrelacement, ces moyens (MD1) déterminant lesdites adresses à partir des valeurs fournies par les moyens de calcul intermédiaires (MCI), les deuxième et troisième compteurs (CT2, CT3), et à partir du paramètre M,

et par le fait que les deuxièmes moyens d'adressage(MDA2) comportent en outre des deuxièmes moyens de détermination d'adresse (MD2) aptes à déterminer les adresses successives de lecture et d'écriture dans ladite mémoire, des données successivement délivrées aux moyens de désentrelacement, ces moyens (MD2) déterminant lesdites adresses à partir des valeurs fournies par les moyens de calcul intermédiaires (MCI), les deuxième et troisième compteurs (CT20, CT30), à partir du paramètre M' et de la taille (OF) du premier espace-mémoire.

INTERNATIONAL SEARCH REPORT

International Application No
PCT/FR 01/02243

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H03M13/27

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H03M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, PAJ, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	VEITHEN D ET AL: "A 70MB/S VARIABLE-RATE DMT-BASED MODEM FOR VDSL" IEEE INTERNATIONAL SOLID STATE CIRCUITS CONFERENCE,IEEE INC. NEW YORK,US, vol. 42, February 1999 (1999-02), pages 248-249, XP000862325 ISSN: 0193-6530 the whole document ---	1,2
Y	US 5 751 741 A (HOEKSTRA GEORGE ET AL) 12 May 1998 (1998-05-12) column 3, line 55 - line 65 column 4, line 29 - line 40 column 5, line 64 -column 6, line 4 --- -/--	1,2

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
25 September 2001	01/10/2001

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	Ogor, M

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INTERNATIONAL SEARCH REPORT

International Application No
PCT/FR 01/02243

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
A	EP 0 856 949 A (ALSTHOM CGE ALCATEL) 5 August 1998 (1998-08-05) column 2, line 10 -column 3, line 21 column 7, line 22 -column 14, line 31 figures 5,6 ---	1-3
A	US 5 912 898 A (KHOURY GEORGE) 15 June 1999 (1999-06-15) column 3, line 23 - line 60 ---	1,2
A	PATENT ABSTRACTS OF JAPAN vol. 1997, no. 02, 28 February 1997 (1997-02-28) & JP 08 265177 A (TOSHIBA CORP), 11 October 1996 (1996-10-11) abstract -----	1

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